PWM Average Models have evolved over time to include mode changes, transport lag near the switching frequency and large signal behavior. Original models did not include both continuous and discontinuous inductor switching. But coming full circle, the modern PWM implementations use synchronous switching to eliminate the free wheeling diodes forward conduction loss. The buck regulator shown in Figure 1 is replaced by the "modern" configuration shown in Figure 2. Inductor current stays in continuous mode when synchronous switching is used. Instead of using complex mode switching average models, the original average model shown in figure 3 can be used. This is an important observation because the simulation speed and convergence is superior for this model. Moreover, the regulator exhibits bi-directional power transfer characteristics. When power is transferred in both directions, a new problem is introduces. The traditional peak current sensing methods fail for negative current, resulting in instability caused by current feedback cut-off.

Average models are slightly different than a standard z-transform representation. That's because the z-transform models events at the switching sample points. If taken at the beginning of the PWM cycle, the Output voltage would be at its minimum value and the average would be larger by ½ the pk-pk ripple. Modeling the average value eliminates the discrepancy. Z-transforms are still used, but they represent what's going on at the "average" sample time.

When using the average model to represent a peak current controlled SMPS, the Duty Ratio can be calculated based on the peak switching value as shown in Figure 3. If the computational plus A/D conversion time is less than the time of the interval between PWL turn-off and average sample time, then performance equal to the "analog" peak current controlled SMPS can be achieved. Notice that division by (vout-Vin) is required. That can by done using Newton iteration rather than successive divide steps. For a 1MegHz switcher, that requires computational delays on the order of 250nsec. That translates to 400mips using our Virtual Current Feedback Controller which is a few years beyond the state-of-the-art in 2009. The numbers work out for a 100kHz switcher; however, the size and cost of the power components is excessive for low poser designs.

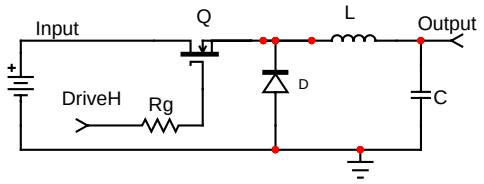


Figure1, Buck Regulator with Freewheeling Diode

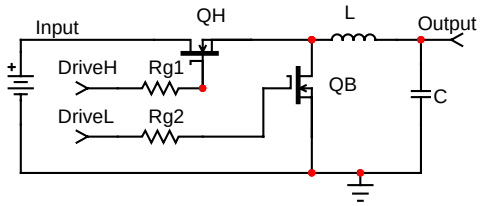
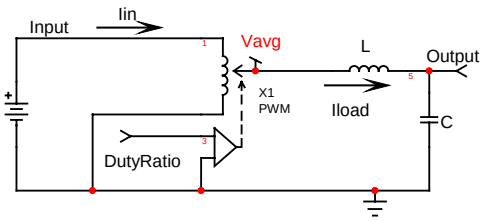
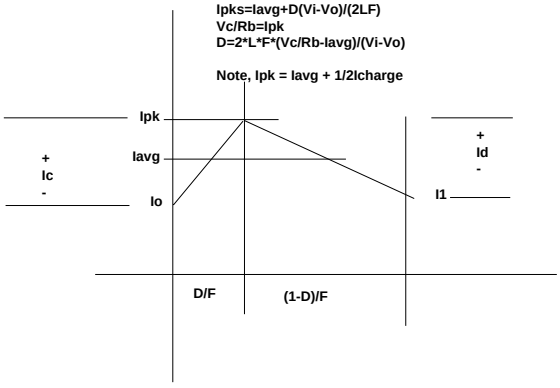


Figure 2, Synchronous Switched Buck Regulator



*Vavg = DutyRatio*Input*
*Iin = DutyRatio*Iload*

Figure 3, Average Model and Equations



Where Vc = Control Voltage
Rb = Burden (Sense) Resistor
D=Duty Ratio
L= Inductance of the switched inductor
F=Switching Frequency

Figure 3, Plot of current vs. time used to derive peak current control equations