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Personal Computer Circuit Design Tools

N E W S L E T T E R

Introduction to interconnects

Whether you design analog, digital, rf or power electronics; parasitic elements control circuit performance. Understanding these effects and accounting for them in a design can separate success from failure. Circuit interconnection or wiring is an important parasitic that is not accurately represented in breadboards. The characteristic impedance and length of interconnects almost always change from breadboard to production. Simulation, using IS_SPICE, can account for these changes long before the actual circuit can be evaluated. Moreover, the circuit and the interconnect medium can be optimized without an expensive iteration.

As electronic technology progresses toward higher levels of integration and smaller geometries, the interconnect will dominate circuit performance. Wirewrap and conventional PC board designs no longer support new Integrated Circuit technologies as they move from MegaHertz to GigaHertz frequencies. Thick film and surface mount PC card technologies compliment the advance in IC technology, but attendant with their benefits is the absence of a simple laboratory verification technique.

Simulation must play an increasing role in the design process because these new microelectronic packages, like their IC counterparts, are difficult to rewire, probe or patch when designs don't work the first time. Achieving a correct or produceable design with minimum iterations is more important now than ever before.

Transmission Line Modeling

The first approach one naturally thinks of for modeling wires is the transmission line. The transmission line model in IS_SPICE has several disadvantages. First, there is no provision for mutual coupling so that crosstalk and ground plane noise cannot be simulated. On the practical side, the second drawback is the large computer memory requirement of the transmission line model.

The transient simulation program must set breakpoints for transmission lines. Breakpoints are absolute simulation times that are stored in a table and result in forcing the simulation program to reach the time specified by the breakpoint exactly. This is done because driving functions and their delayed functions may not contribute to local truncation error, the parameter used to control time steps. The breakpoint table forces a minimum time step required to solve this problem.

The breakpoints must be set for each possible delay arising from driving functions and other transmission lines. The method used to set the breakpoints causes all possible breakpoints to be saved in memory after which redundant breakpoints are purged. If you have two transmission lines in a simulation, then there will be N1*N2/2 breakpoints saved where N1 and N2 are the number of transmission line delays over the analysis for each line. For example, if the analysis of two .5 Nanosecond transmission lines was to run for 100 Nanoseconds, then 200*200/2 or 20000 breakpoints would be saved. Each breakpoint uses 8 bytes making the total memory requirement of 160K Bytes. Most of these would be purged, however, you would be unable to run the problem on a PC because all of the allocated memory would be used just for this calculation. The above example represents a typical interconnect length of 4 inches and the analysis time produces just one cycle of a 10MHz clock.

Even spinning the problem off to a mainframe just postpones the inevitable “out of memory” error since the memory used grows by the square of the analysis time, that is, running the same problem for a 1 Microsecond analysis time will consume 16 Million Bytes, more than is usually allocated on mainframes.

Reworking the IS_SPICE algorithm is being considered; however, the inability to run the same analysis on a mainframe can be a severe handicap for many large circuits. The additional need to account for crosstalk makes an alternative approach desirable.

Lumped L-C Models for Interconnects

The PRE_SPICE version 2.0 library includes a lumped L-C model of a wire or transmission line segment. This model is based on work presented in ref. 1 and standard transmission line equations from ref. 2 and 3. A lumped L-C representation of a transmission line is valid when high frequency components can be neglected. Errors introduced then depend on the terminating resistance and excitation rise time. Reference 1 uses as a rule of thumb a rise time greater than 3 times the single L-C section delay. The delay of a 1 inch interconnect is typically 125P Sec so that rise times greater than 375P Sec would pass this criteria. To get errors down to 1 or 2 percent when compared to an ideal transmission line requires a considerably slower rise time. Data presented in our PRE_SPICE version 2.0 documentation indicate a factor of 10 to 20 is more reasonable.

Interconnect Impedance for Typical Circuits

Many of todays circuits have rise times on the order of 2 Nanoseconds, making a single section valid for 1 to 2 inch connection lengths. Longer runs require more L-C sections. We provide 2 models, a single section in a subcircuit called WIRE and a 4 section model in a subcircuit called WIRE4. In both models we assume a Printed Circuit Card or Wirewrap transmission propagation delay of 125P Sec per inch. Parameters passed to the subcircuit are LEN, the length in inches and Z the characteristic impedance in Ohms. The values of the L-C components are then computed based on LEN and Z using 125P Sec per inch for propagation delay.

Characteristic impedance will usually vary from 50 Ohms up to several hundred Ohms; however, very low impedances are possible for power circuits. Impedances above several hundred Ohms are rare because the impedance becomes a logarithmic function of conductor separation [3] as the separation dimension becomes large compared to the conductor width or diameter. Hybrid technologies using Alumina will reduce propagation velocity and impedance because of the high dielectric constant and small insulator thickness. This is offset to some extent by the shorter interconnect length.

Applying the Model to a Sample Microprocessor

These models have been applied to the following circuit, a clock distribution problem for a small microprocessor Printed Circuit Card. The interconnect schematic, shown in figure 1, includes geometrical relationships. Also shown is a parallel tri-state line for which we will extend the model to measure crosstalk.

The questions we want to explore are:

1. For a series terminated clock driver, what is the effect of series resistance?

2. Should there be any termination at the “end” of the transmission line?

3. What parameters are important for determining crosstalk?

4. Does crosstalk change the clock line waveform?

Of secondary interest is the effect of driving the interconnect with a current source and using a shunt termination at the “end” of the transmission line. Current driven transmission lines are known to be superior from experience with ECL logic, however, they present a higher degree of difficulty for TTL or MOS logic families.

The rising application of integrating communications functions such as phase lock loops or flash A/D converters with digital logic requires an understanding of “noise” coupling into the ground plane. The WIRE model will then be modified to include the ground plane inductance in order to identify the severity of digital signals coupling to analog functions. While these “noise” problems are usually suspected, it may be difficult to convince your project manager to increase the design complexity by including an analog ground plane. Perhaps a simulation would be of some help!

The Clock Distribution Problem

To begin the clock distribution problem, we will assume that the clock driver is a constant impedance driver. While this may not be true for some TTL totem pole drivers, it will simplify the simulation problem. When the “best” terminations are found, the actual driver output stage can be simulated.

Device loads are assumed to be capacitive, about 7PF each, including the package capacitance. It can be seen by inspection of the WIRE subcircuit in figure 1 that this 7PF load will reduce the effective transmission line impedance, causing the best series terminating resistance to be significantly lower than the transmission line impedance. The extra capacitive load will also increase the clock line current, making us suspicious that inductive coupling may be an important crosstalk parameter.

The series terminated transmission line should be well behaved at its output, however, the output reflection will cause a flat spot half way up (or down) the waveform for circuits connected near to the clock driver. The main worry is that negative going transients will cause substrate current to flow in the IC’s, thereby breaking down the junction isolation which eventually leads to logical malfunction or latch-up and device burn out.

Figure 2 shows the first cut, using a 10 Ohm driver with a 3 Nsec clock rise time. The waveforms may represent what you have seen on some Wirewrap backplanes at lower frequencies.

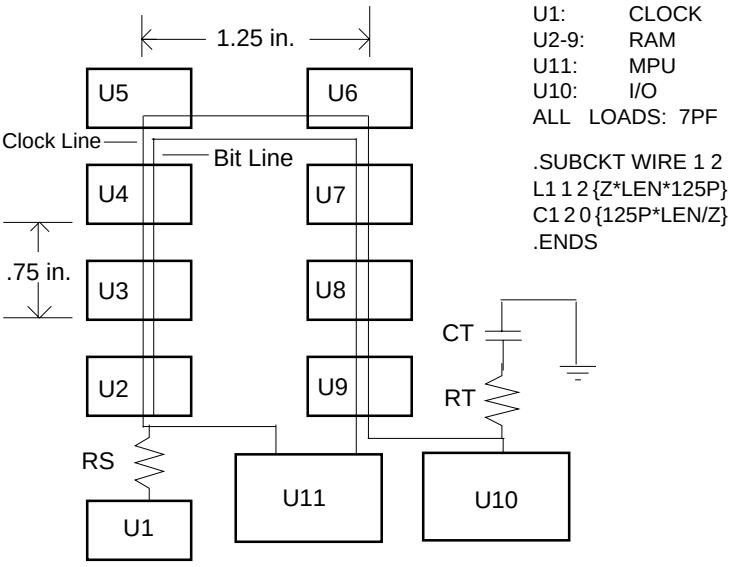


Figure 1 Microprocessor Clock Distribution

Next, figure 3 shows that the best series resistance, 33 Ohms, still leaves an 391mv volt negative undershoot. Placing a series R-C of 68 Ohms and 15 PF at the end of the interconnect virtually eliminates the undershoot as shown in the lower trace, VT(U1). The flat spot in the waveform near the driver should be acceptable, however, it may be worth simulating the response of the IC clock shaping circuit. Clock skew is particularly difficult to determine without modeling some of the internal IC circuitry.

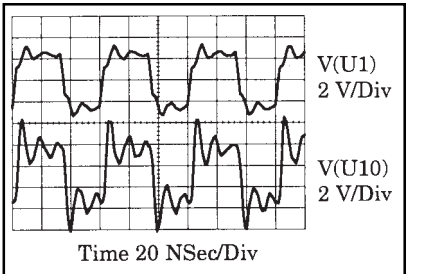


Figure 2 Unterminated Waveforms

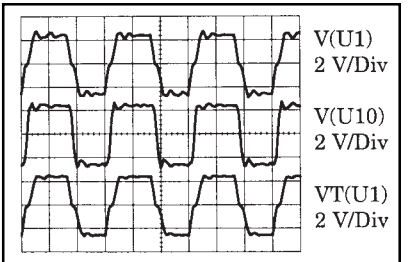


Figure 3 Terminated Waveforms

At this point we have shown that the clock distribution system should leave room for a series terminating resistor if one isn't

built into the driver and that an R-C termination should also be provided. The clock distribution has not accounted for proximity effects which may change the waveform and perhaps adversely affect nearby circuits. one approach is to guard the clock with adjacent grounded traces in order to remove the variability caused by changing impedance in adjacent tri-state traces. Further, it may be necessary to tune the artwork geometry in order to match a fixed resistance clock driver.

Modeling Crosstalk

An adjacent trace will be coupled both capacitively and inductively. A new wire model, MWIRE, is a 4 terminal model for 2 adjacent traces. Shown in figure 4, the capacitive and inductive coupling are both considered proportional to a coupling constants, KC and KM. Applying the same coefficient for both could be rationalized by the inverse square law relationship for both electric and magnetic fields. Clearly, the relationship would be different for adjacent traces on the same plane versus adjacent traces on adjacent planes. This points out the need for some experimental verification for specific applications.

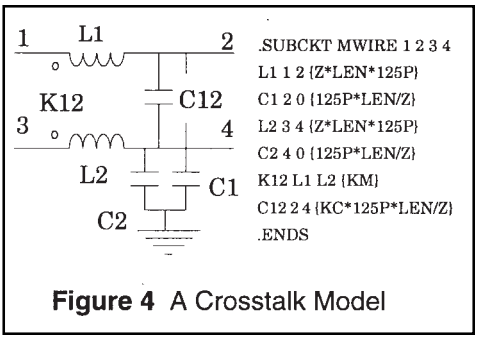


Figure 4 A Crosstalk Model

We will vary the coupling coefficient and even eliminate the magnetic coupling in the following analysis in order to find the effect of crosstalk. This approach will help identify the level of detail needed for experimental verification. One of the effects of interest is to determine the difference between "forward" and "backward" crosstalk. Forward crosstalk is a measure of the unwanted signal when the signal line is terminated near the clock source. Backward crosstalk is the measure of unwanted signal when the signal line is terminated near the end of the clock line. In both cases, the unwanted signal will be measured at the open circuit end of the signal line. We will also see how the loss of energy to the adjacent trace changes the basic clock waveforms. Figure 5 shows the clock, V(U1) and crosstalk

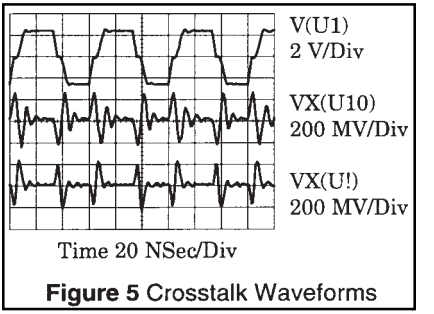


Figure 5 Crosstalk Waveforms

waveforms, VX(U1) and VX(U10) for combined magnetic and capacitive coupling with KC=.1 and KM=.1.

Table 1 summarizes the crosstalk for different coupling coefficients, including a zero magnetic coupling case.

Table 1 Crosstalk in pk-pk volts

KC (1)	KM, Magnetic Coupling Coefficient									
	.00	.02	.04	.06	.08	.1	.12	.14	.16	.18
0.1	.07	.13	.20	.27	.33	.40	.46	.54	.60	.67
0.2	.13	.20	.27	.33	.39	.46	.53	.58	.65	.72
0.3	.19	.25	.32	.38	.48	.51	.58	.65	.71	.78

Note (1): KC is the capacitive coupling coefficient

These results dramatically illustrate the importance of simulating magnetic coupling. Most of the unwanted signal has been inductively coupled on the signal line. The difference between forward and backward crosstalk is seen to be negligible, largely because the crosstalk from magnetic coupling behaves as a series EMF. The clock line waveforms have deteriorated, and in fact the R-C termination could be removed. If this circuit were breadboarded using Wirewrap, the clock waveform damping caused by adjacent wire proximity would have provided damping, while a well constructed PC Card would have much less energy loss to adjacent traces, resulting in potential circuit malfunction from ringing.

Ground Plane Coupling

The MWIRE model can be modified by reducing the inductance in the ground side; for example, by a factor of 20. The potential seen on the ground plane will be maximum directly under the clock line and will diminish as one probes in a normal direction away from the clock trace. Moreover, high frequency signals would propagate near the trace surface causing the problem to be 3 dimensional.We wish to present a simplified one dimensional model, representing the average signal strength along the ground plane. Application of the model requires experimental verification to develop the signal profile in the normal direction.

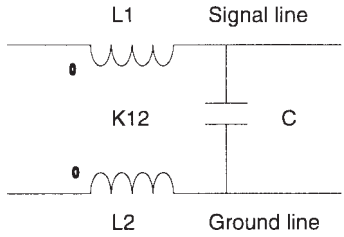
Having seen the importance of magnetic coupling in the crosstalk simulation, it is prudent to introduce the term here. We would like to vary the magnetic coupling coefficient and the effective size of the ground plane along with wire length and impedance. The parameters we have chosen to pass to the model are then:

Z	Characteristic Impedance in Ohms
LEN	Length of a segment in Inches.
K	Coupling Coefficient
N	“Turns Ratio”

The coupling coefficient and turns ratio are borrowed from transformer theory since they relate closely to the coupled inductor model. The coupling coefficient is the ratio of flux linked to total flux and the turns ratio is a function of the ratio of trace width to ground plane width. The coupling coefficient can be quite high which would cause the transmission line impedance to change if all other parameters were to remain fixed. The following equations were used to define L1, L2, and K; the coupled inductor model parameters:

K12 = K, Unchanged
LT = Z*LEN*125P
L1 = LT/[N^2 - K*N + 1]
L2 = L1*N^2

where; C = 125P*LEN/Z



These equations preserve the transmission line impedance while allowing the terms N and K to be varied in the simulation. The coupling coefficient, K, is a function of the ratio of trace size to dielectric thickness. The function can be determined by breaking the problem into a set of small elements and averaging coupling for each pair. The coupling between adjacent ground-trace elements is d/(d+t), where d is the element size and t the dielectric thickness. Coupling to the ground plane will diminish as one probes in the direction normal to current flow. Capacitive coupling will behave in a similar fashion. The problem is to lump or average K for each element to achieve an approximate average for some offset probe position. The ratio, N, is likewise an average of the relative size of the conductor trace to ground plane width. N should decrease as K is decreased since this represents a position further from the signal trace. The simulation we will perform will vary (N,K) from (.01,.5) to (.1,.05) and we will measure the pk-pk signal over a .75 in.

length. This length is approximately the maximum distance between pins on a DIP package. Our main interest is to show that substantial noise, relative to analog circuit performance parameters, is found on the digital ground plane for a wide range of assumptions. Figure 6 shows a typical case for noise across a .75 inch section (K=.3, N=.03) along with the associated clock signal. Table 2 summarizes results for a number of cases. Further experimental and analytical work is needed to define the method for averaging K and N.

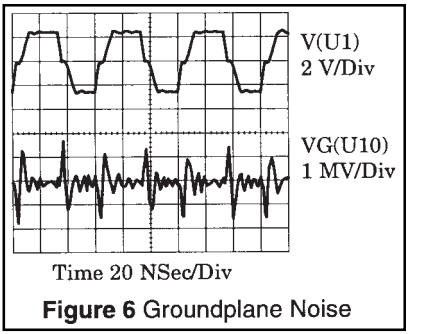


Figure 6 Groundplane Noise

Table 2 Groundplane noise in millivolts pk-pk

	Coupling Coefficient, K				
N	.1	.2	.3	.4	.5
.01	.4	.8	1.3	1.8	2.1
.05	1.2	3.6	5.6	8.0	10.8
.09	1.4	4.9	9.0	13.2	17.5

An ECL Clock Driver

Taking the sample from figure 1, with termination at the end of a current driven clock line and an R-C damping resistor at the clock driver produces substantially better waveforms as shown in figure 7. Clearly, this termination technique will be seen more frequently as GaAs and fine line CMOS technology push clock speed beyond 100 MegaHertz. One advantage of this technique is the reduction of the amount of IC real estate needed to drive a low impedance interconnect. For FET circuits, the Gm of the output device must be on the order of 1/Rt. Even larger Gm's are needed if the IC process cannot produce accurate terminations. The current driver only needs a device that will support the output current, and only in one direction. Practically speaking, this reduces the output driver size by a factor of 10 and its resultant propagation delay

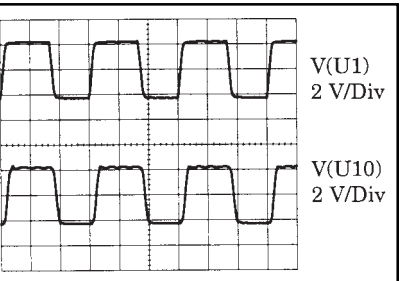


Figure 7 Current mode termination

is less since fewer drivers need to be stacked in series to buffer the internal circuitry from the high capacitance output device.

Summary

Several example have shown the capability of the Intusoft simulation package to predict the effects of interconnect parasitics on digital and analog circuits. The PRE_SPICE models have been extended to account for ground plane noise, however, additional analytical or experimental work is need to evaluate the model parameters for specific applications.

Bibliography

[1] HYBRID CIRCUIT TECHNOLOGY FOR VHSIC
Lewis, E.T.; Ciccio, J.; Thun, R.E.
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1980 Proceedings of the Hybrid Microcircuits Symposium, pp48-93

[2] REFERENCE DATA FOR RADIO ENGINEERS
ITT, 5TH Edition, chapter22, pp22-26
Howard W. Sams & Co.

[3] MICROWAVE CIRCUITS ANALYSIS
AND COMPUTER AIDED DESIGN
Fusco, V.F.
Copyright Prentice Hall, 1987, pp72-73

Correction: The PRE_SPICE Zero Order Hold model, also shown in the Feb., 1986 Newsletter should be changed to the following:

```
.SUBCKT ZOH 1 2
*ZERO ORDER HOLD
RIN 1 0 1E12
E1 3 0 1 0 {K}
T1 3 0 4 0 Z0=1 TD={TD}
RT1 4 0 1
R1 3 5 -1K
R2 4 5 1K
C1 5 2 {TD*1M} IC=0
RC1=1E12
EG 2 0 5 0 -1E6
.ENDS
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The transfer function is:

$$\frac{K(1-Z^{-1})}{TD*s}$$