# Intusoft Newsletter

*Personal Computer Circuit Design Tools*

August 1990




(310) 833-0710 Fax (310) 833-9658

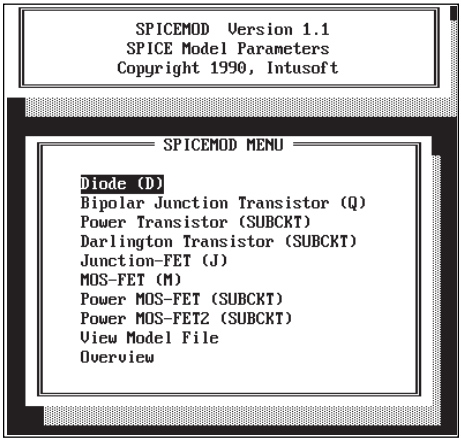
## UNLIMITED SPICE MODELS !!!

Intusoft announces SpiceMod, the Spice Modeling Spreadsheet. SpiceMod is an accurate, easy to use model generation program that allows you to create your own Spice models for: *Diodes (silicon, schottky, zener), Bipolar Transistors, Power Bipolar Transistors, Darlington Transistors (npn, pnp), Jfets (n/p), Mosfets and Power Mosfets (nmos, pmos)*. With SpiceMod you can:

- **Generate max, min, or typical Spice models from common data sheet data.**
- **Make accurate models for most common semiconductors in under one minute.**
- **Automatically store them in the Intusoft library format and ASCII files.**
- **Use the models you create with ANY Spice simulator on any computer.**

**In This Issue**






The difference between SpiceMod and other modeling programs is that you always get realistic dynamic parameters, even if you enter incomplete data. As data is added, the SpiceMod estimates will become more accurate. This provides for a realistic model, always. No tweaking of curves or complex calculations are needed. To use SpiceMod, just select the device type and enter as much data as is available. The more data you enter, the more accurate the model will be. As you enter data, you will see the Spice model update immediately. After entering the data, the model can be saved in an ASCII file (.LIB) and used in your Spice simulation.

# Modeling Pulse Width Modulators

Modeling power electronics, like so many other SPICE applications, requires continuous time models for switching circuits. Just as in our March newsletter on Switched Capacitor filters, the motivation for continuous time models is to eliminate the computationally intensive cycle by cycle simulation, replacing the switching circuitry with a model that averages the switching behavior. Besides being more efficient, the continuous time models allows direct utilization of the AC analysis features of IsSPICE. The IsSPICE program automatically linearizes the model about its nonlinear operating point and provides the data necessary to construct Bode Plots and perform stability analysis.

We have previously modeled a pulse width modulator [1,2,3] that was restricted to operation with the switches in continuous conduction. A great deal of work has been published on the use of this type of PWM model and its simulation limitations [1]. However, while continuous conduction is usually the most severe case for satisfying stability criteria, it would be useful to bridge the gap to discontinuous conduction using one model so that large signal behavior could be simulated.

## A Buck Regulator Model

The buck regulator circuit, Figure 1, is shown in the state of discontinuous conduction. It can be seen that the free wheeling diode, D1, comes out of conduction before the next switching cycle begins. The abrupt change in impedance causes the assumptions regarding the equivalent switch states of the original model to be violated.

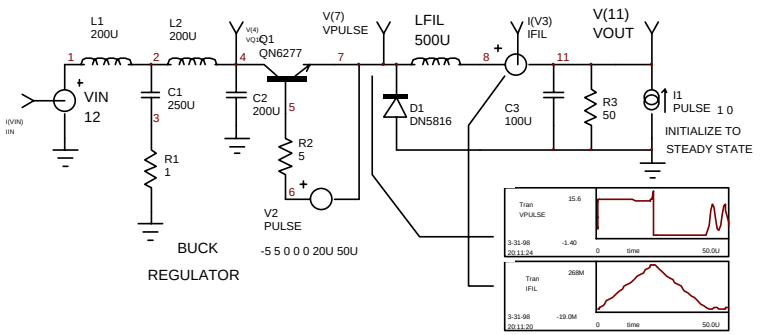



**Figure 1**, A switching model of a buck regulator in discontinuous conduction.

One of the key assumptions required for the use of the continuous time model is that superposition holds. In cases where the circuit impedance varies with time, superposition is invalid and the replacement of a switched value with its duty cycle weighted

average is invalid. To account for continuous and discontinuous conduction, a non-linear model is needed. The new model must account for the changing impedance at the switching terminals.

In this model we will ignore the high frequency ringing and switching noise. Some of these effects could be added back after making the model in order to study the transfer functions and time domain behavior of the input and output filters. For now, we will only look at the continuous time model at frequencies below the Nyquist frequency.

## Developing The Buck Regulator Model

The diagram shown in Figure 2 shows how we went about adding the discontinuous conduction non-linearity. Basically, discontinuous conduction restricts the current flow in the output inductor to be in only one direction. This constraint is satisfied by placing a diode in series with the inductor. Next, it is necessary to account for the minimum value of current that is supplied in discontinuous conduction. The current generator, Imin takes care of this. Notice that when the diode is conducting, the current supplied by Imin does not affect the output waveforms. Its contribution to the input current is taken care of separately. This observation simplifies the computation of the Imin value since we only need to be concerned with the discontinuous case, that is, we only need to provide Imin accurately when D2 < (1 - D1). The modeling equations can then be developed as follows:

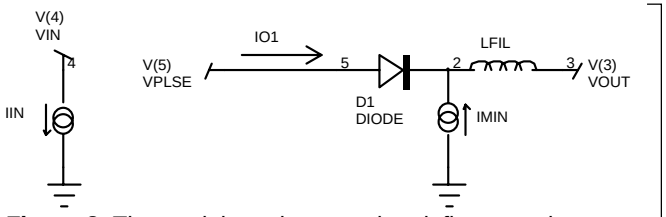



**Figure 2**, The model topology used to define equations.

| Terms: | | |
|---|---|---|
| | D1 | duty cycle for series switch conduction |
| | D2 | duty cycle for commutating diode conduction |
| | D3 | time for no conduction |
| | | (D1 + D2 + D3 = 1) |
| | Lfil | buck regulator filter inductor in Henries |
| | Ipk | change in current during D1 |
| | Iin | regulator input current |
| | Imin | minimum current in LFIL |
| | Io1 | current into the diode |
| | Vin | input voltage |
| | Vout | output voltage |
| | Vflbk | diode flyback voltage (about -.6 Volts) |
| | Freq | PWM Frequency in Hz |
| | Tp | switching period, 1 / Freq |

All currents are in amps and all voltages are in volts.

## Developing The Buck Regulator Model *(con't)*

Using the equivalent circuit of Figure 2, the following equations then define the regulator operation.

$$D2 = D1(Vin - Vout) / (Vin - Vflbk)$$

where D2 is limited to: $0 < D2 < (1-D1)$

$$Ipk = D1(Vin - Vout) / (Freq * Lfil)$$

Then, $Imin = D1 * Ipk / 2 + D2 * (Ipk / 2)$

and $Iin = D1 * Io1 + D1 * Ipk / 2$

The diode is modeled to switch at nearly 0 volts by selecting a small emission coefficient. The concept of a minimum average current is used to define the current in discontinuous conduction. When the minimum current causes the output voltage to be greater than the value produced in continuous conduction, the diode stops conducting and the inductor current becomes the Imin value. The IsSpice subcircuit for the buck regulator, which uses several analog behavioral models from PreSpice, is shown in Table 1. The parameters used to make the subcircuit generic are the switching frequency, filter inductor, and flyback diode voltage. The emission coefficient of the steering diode was chosen to reflect a realistic voltage drop in the series switch. It may be necessary to adjust its value for different circuits.

## Testing The Buck Regulator

The model was tested using the circuit in Figure 3 by comparing results with the switched mode version. First, the duty cycle in the model was adjusted using the CNTRL voltage to match the steady state results (.423V) in order to account for transistor storage time and forward drop. Figure 4 shows a transient simulation which bridges the region, starting in continuous conduction and settling out at steady state in discontinuous conduction. The solid curves are for the switched mode simulation and the dots are the data from Figure 3 using the new model. The new regulator was changed from discontinuous to continuous conduction by pulsing the CNTRL voltage from 0V to .423V.

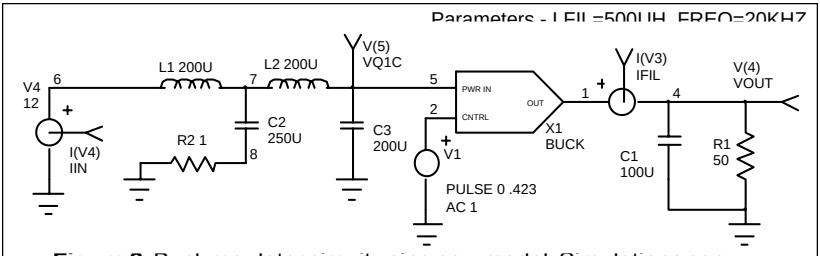



**Figure 3**, Buck regulator circuit using new model. Simulations can be run in both discontinuous and continuous conduction.

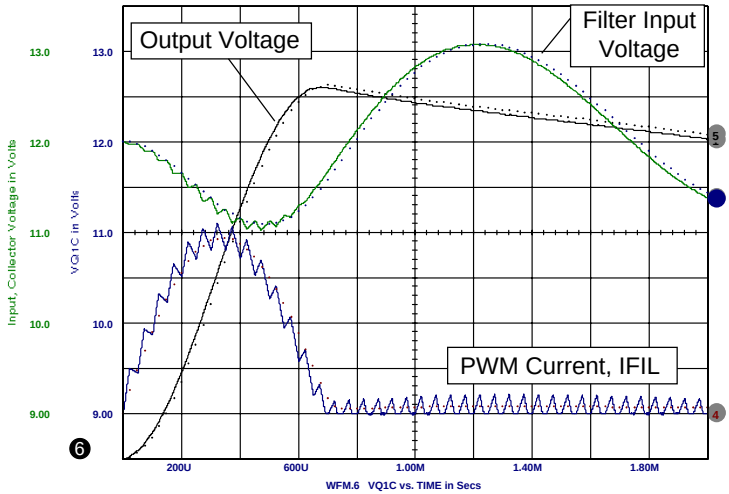
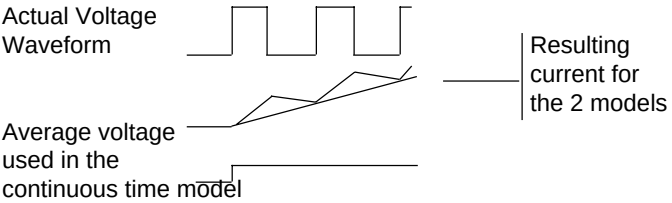


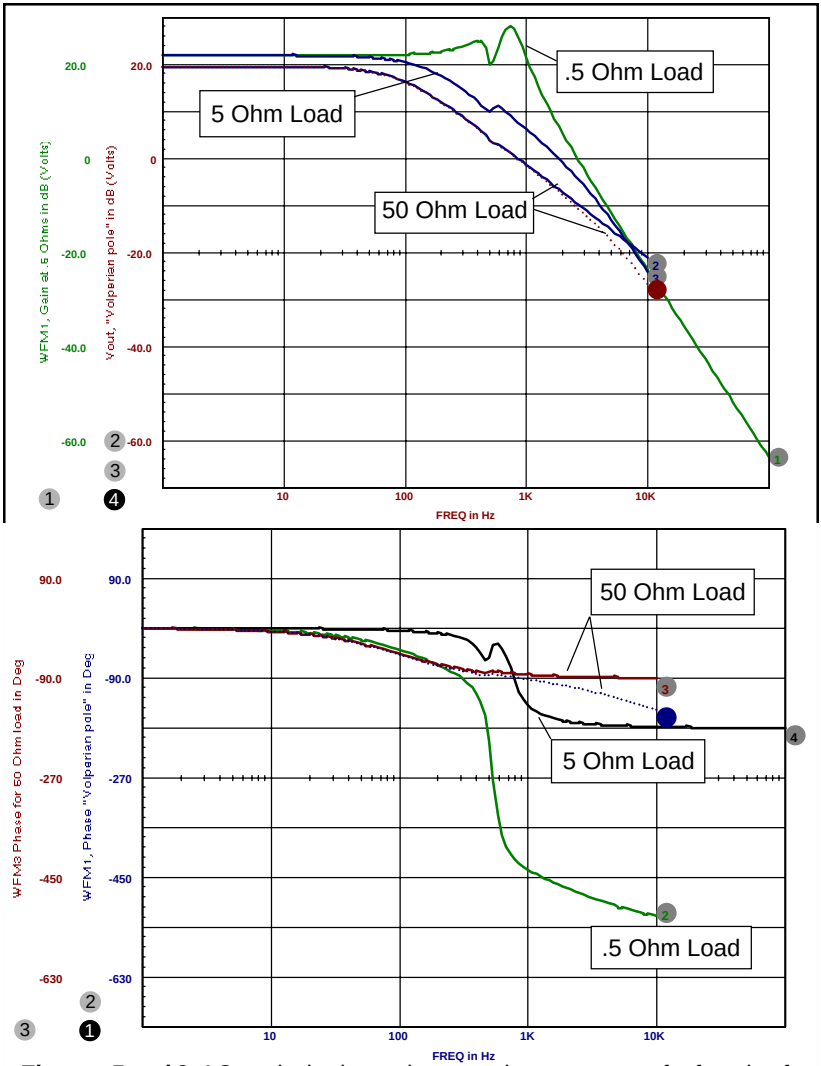

**Figure 4**, Buck regulator transient simulation begins in continuous conduction and transitions to discontinuous conduction at about 300µs.

Notice that the averaging assumption results in a slight displacement in the time domain waveforms because the charge is really delivered by D1 * Tp rather than during all of Tp. The sketch below illustrates this phenomena.




This error is not the same as a delay time error, since phase does not continuously change with time. Realizing that the average actually applies at a slight delay, then the application of Imin to the filter inductor should also be delayed. We were led in this direction because some of our simulations had a discontinuity in voltage at the inductor because the Imin current exceeded the current in the filter inductor after the first sample period. This also makes the current rise and fall time look like the ripple seen in the transient simulation. There are several rationales to select a delay, one of which is to make it a first order lag of Tp / 2. Another placement would make the delay a variable equal to D1 * Tp. We later found that work done by Volperian [4] at Virginia Polytechnic Institute confirms the existence of this pole.

Figures 5 and 6 show the AC analysis for 3 different loads, ranging from discontinuous to continuous conduction, with and without the




**Figures 5 and 6**, AC analysis shows the control to output transfer function for various loads. Magnitude is shown above while phase is shown below.

"Volperian pole". The three loads for the AC analysis were 50, 5, and .5 ohms. Each case used the same duty cycle. Only the 50 ohm load placed the regulator in discontinuous conduction. The heaviest load exposed the interplay with the input filter, showing a potential instability.

Extending this model to other topologies is not quite as straight forward as with the continuous conduction model. For example, a boost topology would require turning the diode around because the free wheeling diode and switching transistor must be interchanged.

To use this model to represent your favorite IC regulator requires that you also include the ancillary circuity associated with the pulse width modulator. Included would be any power switches, rectifier diodes and transformers. The control uses duty cycle normalized so that unity duty cycle is achieved with a 1 volt input. You will have to add the required gain and limiting to simulate the PWM's transfer function. The circuit output at unity duty cycle must equal its input less losses. If transformers are included, this will not be true so that you must also add a “DC” transformer between the input filter and the modulator input. The “DC” transformer is included in our PRESPICE library and discussed in [1]. A typical application for the model is discussed next.

## A 50 Watt Forward Converter

Shown below is the circuit diagram for a forward converter. The portions of the circuit enclosed in the dashed line indicate the functions simulated by the Buck and “DC” transformer models.

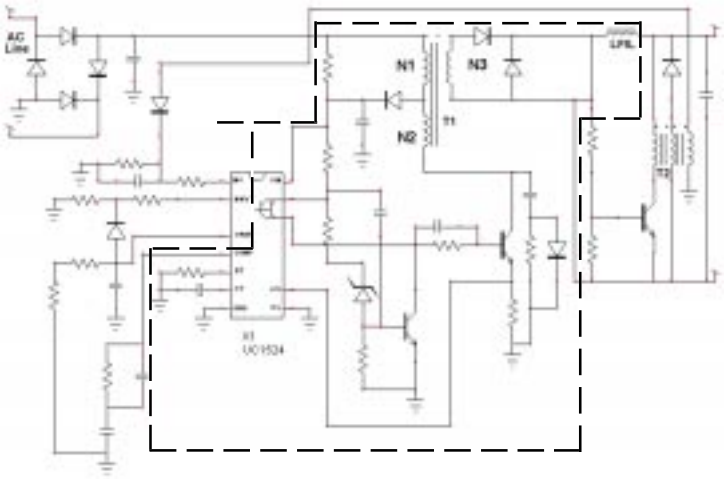



**Figure 7**, Actual forward converter using a UC1524A regulating pulse width modulator. L1's inductor value (40UHY) is used as the LFIL parameter in the buck regulator model.

The corresponding circuit used to simulate the forward converter is shown on the next page. The current limit function is not simulated because a switching analysis is not performed. The feedback network was modeled as a voltage controlled voltage source, E1, with a gain of 1 (equal to the turns ratio of T2). The internal error amplifier was modeled exactly as described in the 1524A's data sheet using simple transistor models with only junction capacitance added. VREF was modeled using a voltage source, while VIN was derived from the input voltage using a Gain

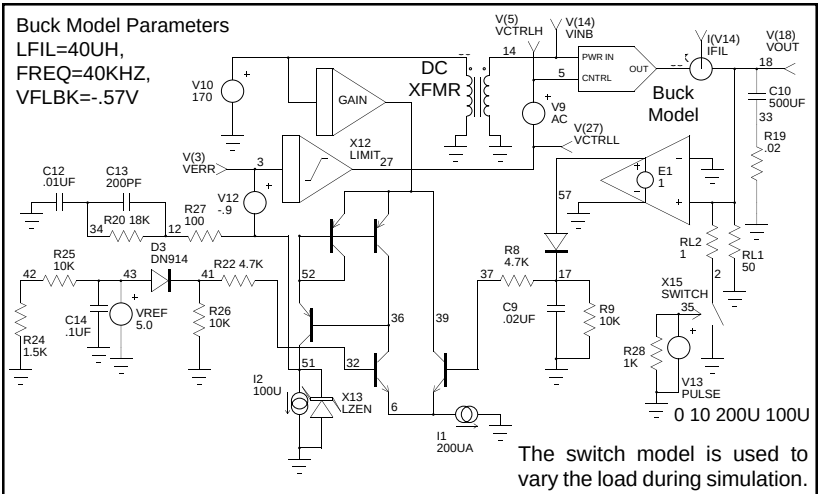



**Figure 8**, Schematic used to simulate the forward converter on page 18-7. The voltage source V12 and Limit function block (gain=.129 for CT=.01UF) convert the PWM transfer function to the 0V/1V - 0%/100% duty cycle transfer function used by the buck regulator model.

block. (Gain=.129=N2/N1). The DC transformer was given a turns ratio of N3/N1. An AC analysis (shown below) revealed the design to be marginally stable (20 degrees phase margin) and very sensitive to the output capacitor's ESR and load impedance. A transient simulation also revealed ringing when the load was changed from 1 Ohm to 50 Ohms and then back to 1 Ohm again. There are a number of methods available to stabilize the regulator including redesign of the feedback network using current feedback.

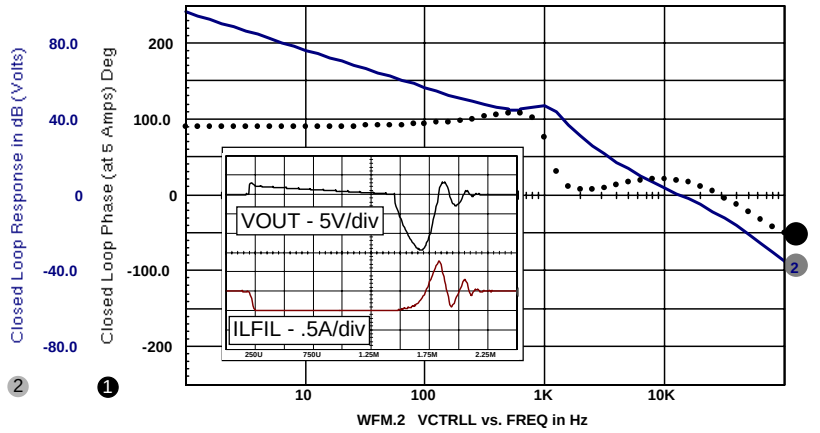



**Figure 9**, AC (Transient inset) analysis of the closed loop response under 1 Ohm, 5A load. The graph was created in IntuScope by subtracting the magnitude(db) and phase(deg) responses at VCTRLH and VCTRLL.

**Table 1**, SPICE subcircuit Listing for the Buck Regulator

```
.SUBCKT BUCK 6        16      25
*                     CNTRL OUT    IN
*PARAMS ARE FREQ(Hz), LFIL (Hy), VFLBK (V)
.MODEL DIODE D(IS=1E-12 N=.42)
X1 6 4 7 1 SUM3A
V2 7 0 1
V3 8 0 {VFLBK }
L1 9 16 {LFIL }
X2 12 4 13 0 LIMITV
X3 6 7 13 SUM2A
X4 4 12 14 SUM2B
E2 15 0  POLY(2) 8 0 4 0 0 0 0 0 1
R2 8 0 1K
G1 0 17 3 0 1
R3 17 0 .01MEG
G2 17 0  POLY(2) 18 0 17 0 0 0 0 0 1
E3 12 0 17 0 10
R4 12 0 1MEG
R5 18 0 1MEG
D1 19 9 DIODE
X5 2 15 11 SUM2C
X6 25 16 20 SUM2B
EX7 3 0 POLY(2) 20 0 6 0 0 0 0 0 {1/(FREQ*LFIL) }
* volperian pole
GG3 5 55 1K
CG3 55 0 {.5M/FREQ }
G3 0 9 55 0 1
X8 21 22 5 SUM2D
X9 3 6 22 MULB
X10 4 3 21 MULB
G4 25 0  POLY(2) 6 0 11 19 0 0 0 0 1K
R6 11 19 .001
G5 0 25 22 0 -.5
X11 8 16 18 SUM2A
E1 2 0  POLY(2) 25 0 6 0 0 0 0 0 1
.ENDS
.SUBCKT LIMITV 1  2   10   11
* PINS ARE    IN OUT +LIM -LIM
*PARAMETERS ARE NONE
RIN 1 0 1E12
E1 3 0 0 1 1
RC1 2 4 .1MEG
C1 2 4 1F IC=0
R1 3 4 .1MEG
E2 102 0 0 4 1E6
DX 102 2 DN
RN 11 0 1MEG
DN 4 102 DN
.MODEL DN D(IS=1E-12 N=.14319)
EP 2 6 10 0 -.0597 1
DP 6 4 DN
.ENDS
.SUBCKT SUM3A 1 2 3 4
* 3 PORT SUMMER
RIN1 1 0 1E12
RIN2 2 0 1E12
RIN3 3 0 1E12
ROUT 4 0 1E12
E1 4 0 POLY(3) 1 0 2 0 3 0 0 -1.0000
+  -1.0000  1.0000
.ENDS
.SUBCKT SUM2A 1 2 3
RIN1 1 0 1E12
RIN2 2 0 1E12
ROUT 3 0 1E12
E1 3 0 POLY(2) 1 0 2 0 0 -1.0000
+  1.0000
.ENDS
.SUBCKT SUM2B 1 2 3
RIN1 1 0 1E12
RIN2 2 0 1E12
ROUT 3 0 1E12
E1 3 0 POLY(2) 1 0 2 0 0 1.0000
+  -1.0000
.ENDS
.SUBCKT SUM2C 1 2 3
RIN1 1 0 1E12
RIN2 2 0 1E12
ROUT 3 0 1E12
E1 3 0 POLY(2) 1 0 2 0 0 1.0000  1.0000
.ENDS
.SUBCKT SUM2D 1 2 3
RIN1 1 0 1E12
RIN2 2 0 1E12
ROUT 3 0 1E12
E1 3 0 POLY(2) 1 0 2 0 0 500.00M 500.00M
.ENDS
.SUBCKT MULB 1 2 3
RIN1 1 0 1E12
RIN2 2 0 1E12
ROUT 3 0 1E12
E1 3 0 POLY(2) 1 0 2 0 0 0 0 0 1.0000
.ENDS
```

## Conclusions

In summary, a model has been developed that can simulate PWM circuits in continuous and discontinuous conduction. This represents a break-through in the simulation of switching power supplies as two separate models were required before. The new buck regulator model allows AC (gain/phase, stability vs. load) and transient (variation of load impedance) analyses to be performed in a wide variety of applications. The model can also be extended to other regulator topologies. The actual model and schematic of the buck regulator, the test circuits, and the forward converter circuits are available to interested users.


[1] "SIMULATING WITH SPICE", Meares, L.G.; Hymowitz. C.E., Intusoft, 1988,
[2] "PRESPICE User's Guide", Intusoft, 1990
[3] "New Simulation Techniques Using Spice", Proceedings of the IEEE 1986 Applied Power Electronics Conference, pp. 198-205
[4] "Simplified Analysis of PWM Converters Using the Model of the PWM Switch", IEEE transactions on AES, March 1990.