

Intusoft Newsletter

Personal Computer Circuit Design Tools

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PRE SPICE UPDATE - OVER 1000 NEW MODELS !

PRESPICE, the SPICE pre-processing program from Intusoft, has been updated to include over 1000 new SPICE models. Highlights include new models for commonly used JEDEC numbered parts from vendors like Motorola, Siliconix, Unitrode, I.R., Harris, SGS-Thomson, and National Semiconductor, and a wide variety of European parts from Philips and Siemens. Also included are several new model types that are not generally available from any EDA tool vendor such as:

- IGBTs
- Fuses
- MOVs
- 555 Timer
- ECL/MECL/CMOS/TTL logic gates
- Switched Capacitor ICs
- Current-Feedback Op-Amps
- Darlington Transistors
- Voltage Regulators
- Vacuum Tubes
- UJTs & PUTs
- Mechanical elements
- Dual-Gate Mosfets

Along with the PRESPICE model libraries, Intusoft's special RF Device Library, and the hardware vendor supplied op-amp model libraries, Intusoft now offers over 1600 models. No other EDA tool vendors can match the combination of model variety, comprehensiveness, and price. All of the models are compatible with any Berkeley SPICE 2G.6 compatible simulator including Intusoft's ISSPICE 1.41 program.

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"A SPICE COOKBOOK" DEBUTS

Intusoft has introduced a new reference book dealing with the analog circuit simulation program SPICE. The book, entitled "A SPICE Cookbook" contains over 100 practical examples encompassing a wide variety of disciplines in the electrical engineering field. Over 225 pages of information allow each circuit example to include a complete technical explanation, related equations and background information, circuit schematic, associated ISSPICE netlist, and resulting circuit output graphs.

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PRESPICE Update Offers Over 1000 Models (from pg. 22-1)

In addition to the part types stated on the previous page, PRESPICE 3.0 also includes models for:

Diodes (Schottky, PN, Germanium, Rectifier, Switching, Varactor, Zener, Laser), Diode Bridges, Transistors (NPN/PNP), Power Transistors (NPN/PNP), JFETs (N/P Channel), small signal MOSFETS (N/PMOS), Power MOSFETS (N/PMOS), Op-amps (Bipolar, JFET), Comparators, Analog Behavioral Models (Mathematical blocks, Ideal Filters, Z and S domain functions), Crystals, Opto-Isolators, Pulse Width Modulators, Buck Regulators, SCRs, Switches, Potentiometers, Transmission lines, Nonlinear Magnetics, Transformers, Thermistors, Neural Network models and more.

PRESPICE: A Modeling Breakthrough

PRESPICE represents a modeling breakthrough for SPICE users for several reasons. Not only does this library provide models that are difficult to find anywhere else, but it also does so at an unbelievably low price. Considering the fact that SPICE modeling services charge between \$200 and \$1000 dollars for a single diode or BJT model, the PRESPICE library represents an unprecedented value. All of the models are strictly Berkeley SPICE 2G.6 compatible and are guaranteed to run on any SPICE compatible program on any computer platform. In addition, the PRESPICE models do not require any extra expensive options, such as the Analog Behavioral modeling option required by some other simulation companies.

How does Intusoft do it? Intusoft is the world's leader in SPICE macro modeling, especially when it comes to documenting, publishing and teaching the world about SPICE modeling through the *Intusoft Newsletter*. Intusoft is also the only vendor that consistently publishes newly developed SPICE models for free. As part of Intusoft's service policy, Intusoft makes models for its customers every day. Through hours of testing and simulation by knowledgeable engineers with years of SPICE modeling experience, Intusoft has been able to accumulate the hundreds of accurate models that are being released in the PRESPICE update. Best of all, Intusoft has kept the price of PRESPICE in line with its policy of making simulation tools available at an affordable price.

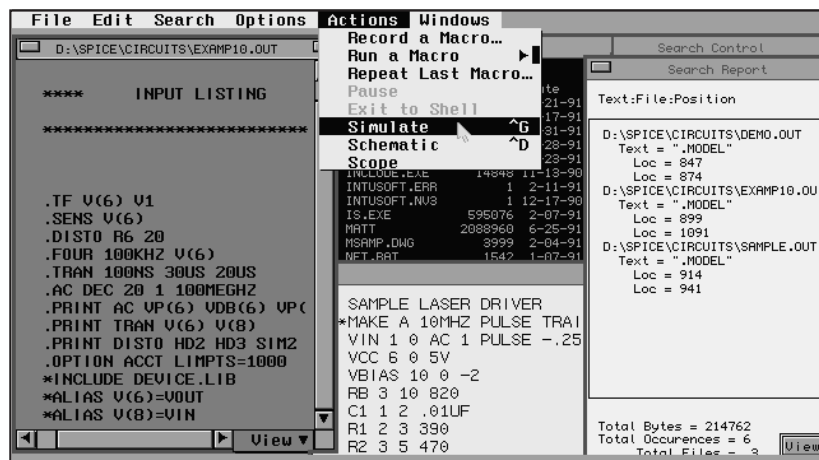
Generic Models Libraries Expanded

Unique to PRESPICE are various generic models which can convert data sheet parameters into SPICE parameters. With the generic models the designer can get a good model for many different types of components even if they are not specifically listed in the

library. PRESPICE contains generic models for diodes, transistors, power transistors, saturable cores, transformers, zeners, fuses, and analog behavioral models to name a few. Over 100 different types are included, capable of simulating thousands of components. Other advanced modeling features such as parameter passing into subcircuits, nonlinear equation based models and function definition statements are also included in PRESPICE.

The majority of the models in PRESPICE utilize custom subcircuit structures developed by Intusoft's technical staff. This is opposed to the traditional method, used by many other model vendors, of trying to model complex electronic devices with only the built-in SPICE primitive elements. The subcircuit approach results in a more accurate SPICE model that better mimics the actual device performance because higher order effects (package parasitics, nonlinear behavior) can be better accounted for. All of the models in PRESPICE are viewable and changeable by the user. Each has been thoroughly tested and verified. Complete documentation including technical descriptions, features, and schematics are provided.

New IsEd Editor Adds Search/Edit Features



Another new module included in PRESPICE (PC version only) is the Intusoft text editor, IsEd, which has been especially adapted for editing and viewing multiple IsSPICE netlists and large library files (Shown left). New features include: ability to open, view, and edit over 20 files at a time, edit large files (>3 megabytes), search, find, and replace text in any file, view DOS directories, and on-line context sensitive help for IsSPICE and PRESPICE. For IsSPICE (PC) users, PRESPICE also adds Monte Carlo Analysis, Parameter Sweeping, and Circuit Optimization capabilities.

“A SPICE Cookbook” Debuts (from pg. 22-1)

In addition, many of the examples include a special “Circuit Specifics” section. This section fully details any IsSPICE simulation tips and analysis techniques encountered during the simulation of the circuit, providing novice, as well as advanced users, deeper insight into the simulation process. Several BASIC programs are also included to enhance the description of the circuit concepts.

Examples Perfect For Engineers/Teachers

“A SPICE Cookbook” is perfect for engineers, novice SPICE users, teachers and students. It contains a wide variety of practical examples which can be used as a guide for future simulations. For example, the sections on transformers, filters, and rectifiers are perfect for those wishing to simulate power supplies. The comprehensive set of topics covers the full range of engineering disciplines (RF, Power, Filter, Digital, Microwave).

In-depth descriptions of basic SPICE simulation techniques are presented throughout the book. Common simulation problems and scenarios including circuit initialization, convergence, SPICE syntax pitfalls, device modeling, and proper circuit partitioning are explained as they are encountered. SPICE models, covering the majority of the components used in engineering classes and college level laboratory experiments, are also utilized throughout the book. “A SPICE Cookbook” provides an excellent source for teachers developing class assignments and guidance for students looking for class projects and help on the intricacies of simulating with SPICE.

Some of the topics in “A SPICE Cookbook” include:

Analog Techniques; Amplifiers, Waveform synthesis, Oscillators, Active/Passive Filters, Transformers, Power Supplies, Signal Processing, Electro-Acoustics

Digital Techniques; Logic Circuits, Multivibrators, Counting Circuits, Digital Signal Processing

Analog Computing; Building blocks, Solving Differential Equations, Neural Networks

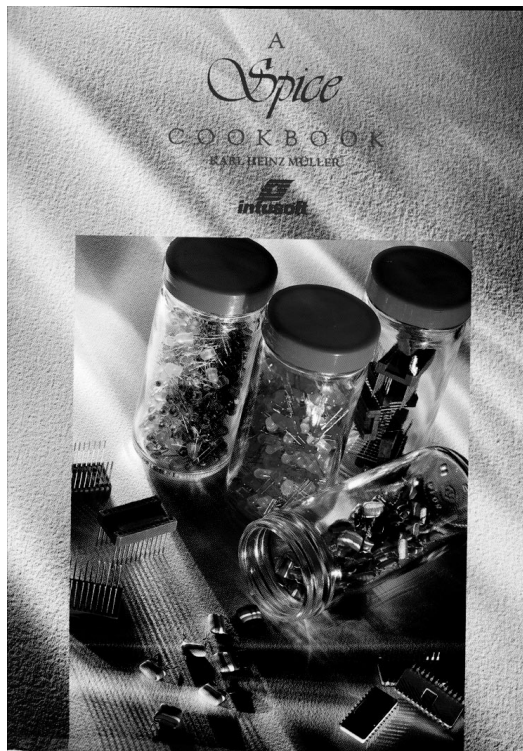
Continuous and Discontinuous Systems; Digital Filters, Noise Generation, Control Systems

High Frequency and Microwave; Couplers, Filters, Mixers, Microstrip networks, GaAs FETs, Antennas

Ordering Information

"A SPICE Cookbook" joins the rest of Intusoft's line of SPICE related publications. The SPICE reference and tutorial guide, "SIMULATING WITH SPICE", and the modeling and simulation text in the "SPICE APPLICATIONS HANDBOOK", perfectly complement the practical examples contained in "A SPICE Cookbook".

Orders for "A SPICE Cookbook" authored by Karl Heinz Muller, may be placed starting August 26, 1991. The book includes a floppy disk with all of the SPICENET schematics, IsSPICE compatible circuit netlists, and SPICE compatible models. Special University discounts are available.



SPICEMOD Helps Model Dual-Gate Mosfets

The dual-gate Mosfet has certain advantages that make it attractive for RF applications, most of which could be effectively simulated by IsSPICE if a suitable model was available. However, due to limitations in data sheet data, it is difficult to create an accurate SPICE model. SPICEMOD, the SPICE spreadsheet modeling program, is fortunately very adept at producing accurate SPICE models from limited amounts of information. And with its help, a dual-gate (D-G) Mosfet subcircuit model can be produced which can then be simulated and optimized using IsSPICE.

Structure and Performance

A DG mosfet is essentially a series arrangement of two separate channels, with each channel having an independent gate connection to control the flow of current (Figure 1).

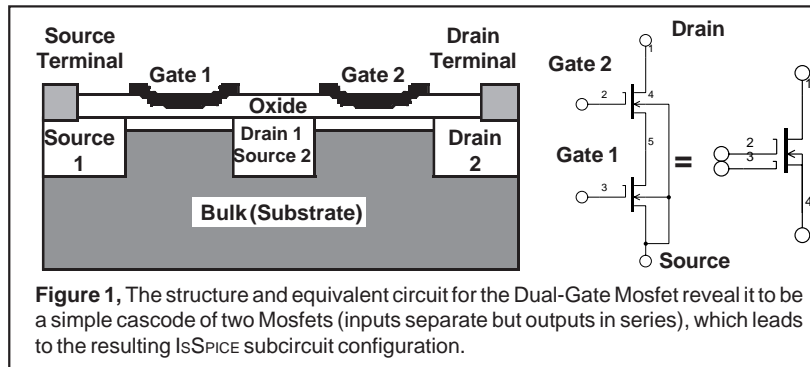


Figure 1, The structure and equivalent circuit for the Dual-Gate Mosfet reveal it to be a simple cascode of two Mosfets (inputs separate but outputs in series), which leads to the resulting IsSPICE subcircuit configuration.

The arrangement results in substantially lower feedback capacitance (C_{rss}), higher transconductance resulting in greater power gain, high input impedance permitting remote AGC capability and improved noise figure over that of single gate devices (Table 1).

Parameter	Dual-Gate Mosfet	Single-Gate Mosfet
C_{rss}	.03 - .05Pf	.1 - .3Pf
Y_{fs}	10 - 20m	7.5m
Power Gain	15 - 30dB	15 - 20dB

Table 1, The differences in characteristics between dual and single gate Mosfets reveal some of the reasons behind the dual-gate Mosfets' inherent advantages.

The availability of two independent control gates on the D-G Mosfet offers unique advantages for chopper, clipper, and gate amplifiers, or for applications involving the combination of two or more signals, such as in mixers, product detectors, color demodulators, and balanced modulators.

Using SPICEMOD To Model D-G Mosfets

Most data sheets do not provide sufficient information to model D-G Mosfets and certainly do not give any insight into converting what data there is into IsSPICE parameters. In this case, the SPICEMOD program can be of tremendous value. SPICEMOD is capable of taking in the data sheet parameters that are normally available, such as VGS(off), IDSS, Yfs, Ciss, and Coss, and creating a realistic Mosfet model for each section of the dual gate device. In Figure 2, we see the SPICEMOD input screen for the Motorola 3N201, chosen because data sheet curves were available for comparison. The data sheet parameters are input for each Mosfet channel, resulting in two IsSPICE .MODEL statements. Combining the SPICEMOD Mosfet models into a subcircuit structured as in Figure 1 is then a simple matter as

```

SPICEMOD 1.4 ===== MOS-FET (M) ===== 06-24-1991

.MODEL Name (M2M4351) = 3N201      (Estimated Data)
.Channel Type (M,P) = NMOS       (Entered Data)
.Enhancement or Depletion Mode (E,D) = Depl
.Max. Drain-Source Voltage, V(CB)IDSS = 25.000 U. <IS>
.Maximum Drain Current, ID = 0.050 A. (Scales all Values)
.Gate Threshold Voltage, VGS(Th) = -1.500 U. <VTO>
.On Resistance, rDS(on) = 60.000 ohms <RD> (RS)
.Forward Transfer Admittance, Yfs = 12.000 mahos <KP>***
.Input Capacitance, Ciss = 3.300 pF. <CIBD>***
.at VGS = 15.000 U.
.Reverse Transfer Capacitance, Coss = 0.014 pF. <CIBD> (CIBD)***
.at VDS = 15.000 U.
.Drain-Substrate Cap., Cd(sub) or Coss = 1.700 pF. <CIBD> (CBS)
.at VD(SUB) = 15.000 U.

*** CAUTION - SEE F1 HELP

===== SPICE MODEL PARAMETERS: =====
.MODEL M3N201 NMOS CLEVEL=1 VTO=-1.5 KP=12.0M GAMMA=7.26U
+ FHI=.75 LAMBDA=3M RD=0.4 RS=0.4 IS=25F PB=.8 NJ=.46
+ CBD=6.64P CBS=7.97P CIBD=160P CIBD=140P CIBD=32.6M)
** - Assumes default L=100U V=100U -
* 25 Volt .05 amp 60 ohm Dep-Mode N-Channel MOS-FET 06-24-1991
<< SELECT WITH ARROWS, ENTER NEW DATA - F1 HELP - 'Esc' WHEN DONE >>

```

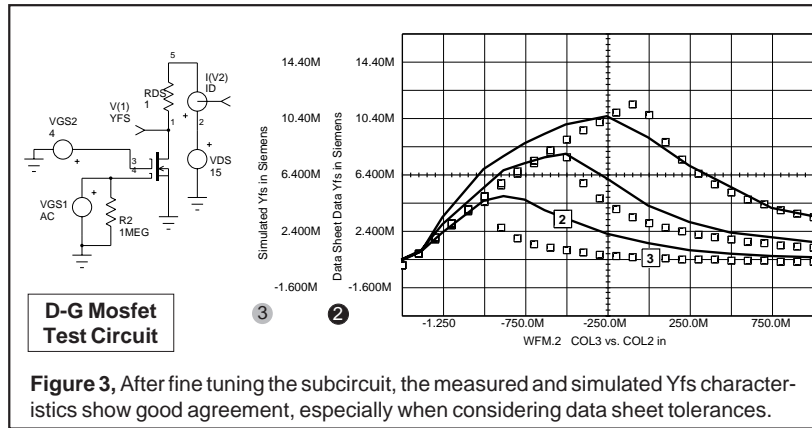
Figure 2, SPICEMOD is used to create the Mosfet SPICE models (3N201-1/-2) used in the D-G Mosfet subcircuit.

shown in Table 2, on the next page. Notice that the source resistance of the gate 2 device and the drain resistance of the gate 1 device are set close to zero in order to achieve the fabricated semiconductor connection. The diode input protection, available on some devices, is not included in the subcircuit model because the resistance is negligible and little capacitive loading is added (<.01-.02PF).

Testing The Models

To test and optimize the D-G Mosfet subcircuit, a simulation was used to generate the ID vs. VDS/ID vs. VGS1 and |Yfs| vs. VGS1 curves. Yfs is defined as the magnitude of the common-source forward transfer admittance and is the most important dynamic parameter for Mosfets. The parameters that had the most effect on the Yfs and ID vs. VDS curves were VTO, KP, and resistances RS and RD. The values generated by SPICEMOD produced good results. However, a greater difference in the thresholds (VTO) of the two Mosfets, than indicated by the typical data sheet values, was required in order to match the Yfs curves. Due to the fact that the individual Mosfets are not symmetrical, the size of the gate 2 channel was reduced (W=35U) from the default 100U value. Also, since the rDS on value was not given, the values for RS and

Testing The Models (cont'd)



RD also had to be adjusted. The differences in VTO, KP and the width, produce the “quasi-saturation” effect similar to power bipolar transistors, as well as, control the position of the peaks in the Yfs curves. Again, noting the wide variation allowed by the data sheet values, the model performs quite well. Large variations in the DC/Yfs response curves were produced in IsSPICE test simulations, in spite of the fact that key parameters remained well within data sheet tolerances, indicating that a great deal of optimization of the DC performance is not warranted.

Conclusions

Though not shown here, an oscillator circuit was also constructed and simulated revealing the transient performance of the new model to be excellent. With the help of SPICEMOD, the creation of accurate D-G Mosfet models is possible. In fact, a library of dual-gate devices from Motorola, Simens, and Philips is available as part of the PRESPICE update. All of the test circuits and schematics from this newsletter are available on floppy disk along with models for the 3N201, BF933, and BF980A devices for \$20.

D-G Mosfet Model Listings and References

Table 2, SPICE Compatible Subcircuit for a Dual-Gate Mosfet

```
.SUBCKT MN201 1 2 3 4
*Connections Drain Gate2 Gate1 Source, * Motorola N-Channel Depletion DG-MOSFET
MD1 5 3 4 4 MN201-1
MD2 1 2 5 4 MN201-2 W=35U
.MODEL MN201-1 NMOS (LEVEL=1 VTO=-1.45 KP=11.8M GAMMA=3.26U PHI=.75 LAMBDA=30M RD=.1
+ RS=24.8 IS=25F PB=.8 MJ=.46 CBD=6.64P CBS=7.97P CGSO=168P CGDO=140P CGBO=32.6N)
.MODEL MN201-2 NMOS (LEVEL=1 VTO=-1.02 KP=12.8M GAMMA=27.26U PHI=.75 LAMBDA=37M RD=22.3
+RS=.2 IS=30F PB=.8 MJ=.46 CBD=6.64P CBS=7.97P CGSO=168P CGDO=140P CGBO=32.6N)
.ENDS
```

- [1] “Computer Simulation of Electronic Circuits”, Raghuram, R., John Wiley & Sons, 1989
 [2] “Manual for MOS Users”, Lenk, John D., Reston Publishing, 1975

Undocumented IsSPICE Options

In this section we will continue our discussion of undocumented SPICE options with a review of some hidden features in the DC analysis. The IsSPICE .DC statement is used to examine a circuit's DC operating point while varying the DC values of one or more voltage or current sources. The syntax is:

```
.DC Source_Name Starting_value Final_value Step_value
```

For example, `.DC V1 0V 10V 1V`, will cause the voltage source named V1 to be swept from 0V to 10V in 1V steps. At each step, the DC values listed in the `.PRINT DC` statement will be saved.

Sweeping Resistors and Temperature

Although undocumented, the `.DC` statement in most Berkeley SPICE 2G.6 compatible programs can also be used to sweep resistor values and the circuit temperature. Even though these and virtually any other variable can be swept using the Circuit Optimizer in PRESPICE, this is an extremely useful feature because it allows the designer to quickly examine the effects of resistance and temperature variations on a circuit's operating point. The syntax required to execute a temperature or resistor sweep while performing a DC analysis is shown below.

```
.DC Resistor_Name Starting_value Final_value Step_value  
.DC TEMP Starting_value Final_value Step_value
```

In addition, the resistor/temperature sweeps can be combined with each other or with the voltage/current source specifications in order to get a more dynamic response from the circuit. This is done by repeating the syntax shown above, for a second reference designation, in the same `.DC` statement. For example:

```
.DC R1 1K 100K 1K TEMP 0 100 25  
.DC R1 10 50 10 V1 0V 10V 1V
```

The statement above would cause the resistor R1 to be swept from 10 to 50 ohms in 10 ohm steps. For each value of resistance, the voltage source V1 would be swept from 0 to 10 volts in 1 volt steps, thus creating a family of curves. At each resistance/voltage combination, the DC operating point would be calculated. The resulting syntax, taking into account the new options for the `.DC` statement is:

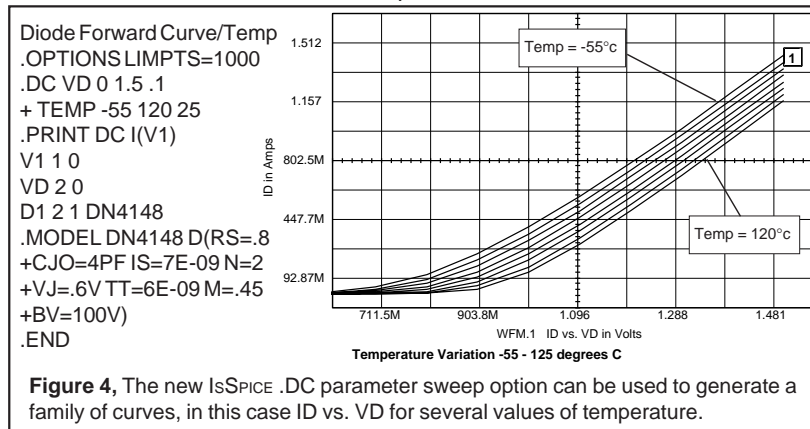
```
.DC RNAME or VNAME or INAME Starting_value Final_value Step_value  
+RNAME or VNAME or INAME or TEMP Starting_value Final_value Step_value
```

Sweeping Resistors and Temperature (cont'd)

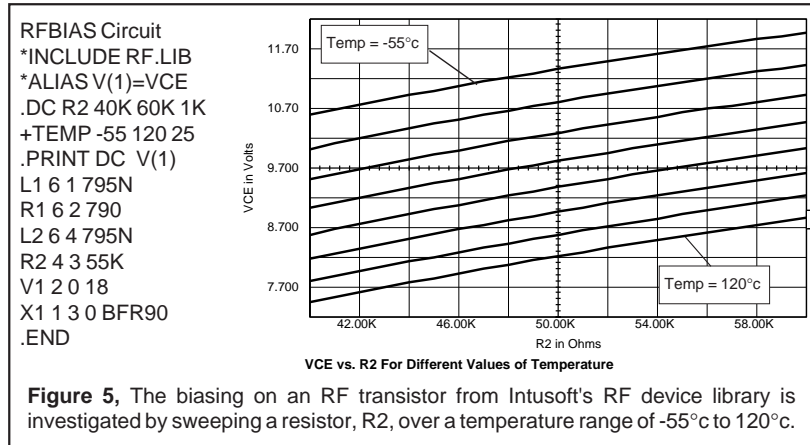
Note that for temperature, the exact word "TEMP" must be used. Also, if temperature is swept, it must be stated as the second variable in the sweep set.

Using The .DC Options

Below are various circuit netlists that demonstrate the use of this undocumented option. The circuit below sweeps a voltage source at different temperatures.



The circuit below sweeps a bias resistor through its calculated value over a temperature range to examine the effects on the value of VCE.



From the above examples you can see that the undocumented .DC sweep options can be a very powerful asset to the already powerful analysis capabilities of IsSPICE. This function can be used to generate a variety of curve families for a DC analysis with great ease.