Intusoft Newsletter

Personal Computer Circuit & System Design Tools

intusoft

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NEW DESIGN VALIDATOR™

Circuit simulation is an iterative process where different aspects of the circuit are varied in order to investigate behavior, improve performance and enable a better understanding of a design. Yet, in spite of this process most SPICE based products still use a batch style of operation. A circuit is simulated and then, repetitively, the results are analyzed manually.

Continued on pg. 2

In This Issue

SPICENET UPDATE AVAILABLE

The new SpiceNet program is designed to make SPICE easier to use than ever before, while still providing a wealth of uncompromising features for the power user. Many new fea-

Continued on pg. 6

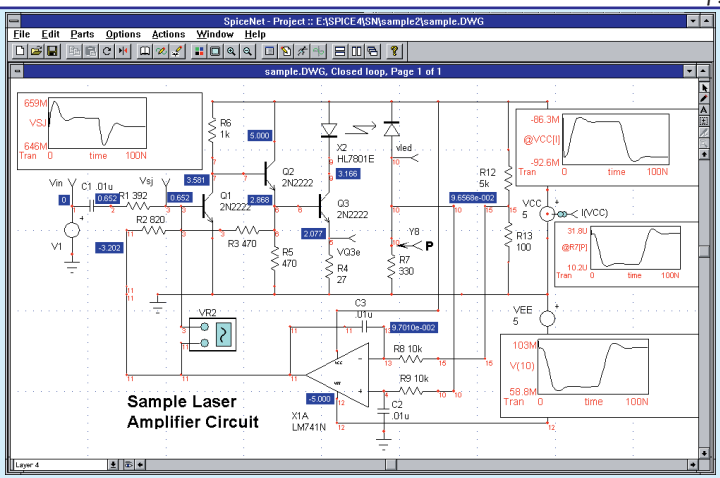


Figure 1, The new SpiceNet schematic entry program is posted for FREE on the Intusoft web site. See page 6 for more details!!

NEW OPTION SUPPORTS DESIGN TESTING

Continued from page 1

Thanks to Design Validator™ this manual, tedious and time consuming paradigm is about to change. Simply put, Design Validator keeps track of multiple Circuit Configurations, Simulation Setups and Measurements. It then runs an entire suite of tests **automatically**. When complete, Design Validator creates a report that summarizes the measurements and pass-fail grades. This powerful capability extends SPICE well beyond its current single simulation oriented boundaries. Contact Intusoft or your local dealer for prices. Design Validator™ requires ICAP/4Windows version 8.1 and will be available May 1, 1997.

How Design Validator Works

You begin by using ICAP/4 to capture different circuit configurations or variations. For example, the amplifier shown in Figures 1 and 2 has two variations; closed loop and open loop. The core circuitry, highlighted in Figure 2, is in both configurations. The difference is the test circuitry which is used to generate the different test scenarios. Each circuit configuration may have a different set of values or be a different design altogether.

Design Validator allows each circuit configuration (Table 1) to be combined with one or more sets of IsSpice4 analyses, also called Simulation Setups. The combination of a Simulation Setup and a circuit configuration is referred to as a “Test”.

Figure 3 illustrates the 4 analysis/configuration pairings. We will look at 2 here; Closed Loop + Standard and Open Loop + Bode Plot. In the first test, we will run operating point, AC, and transient analyses, but only an AC analysis in the second.

Measurements are then assigned to each test. The measurements can be made on any number of nodes or devices, and are setup using an easy-to-use Wizard approach. For the closed loop test, we will record several operating point voltages and the transient characteristics (Max, Pk-Pk) of various waveforms. For the

Design Validator - Uses and Benefits

- Automatically validate and evaluate circuit or model changes against design specifications
- Provide a framework for automatic test set software design
- Make automated design comparisons and measurements, under a variety of conditions

Design Validator - Features

- All Operations Graphically Driven
- Report with pass/fail indicator and measurement results
- Keeps track of different test configurations, measurement tolerances and scenarios
- Automatically performs a variety of measurements on each test configuration
- Quick edit allows you to make circuit changes and resimulate to see a comparison of the results

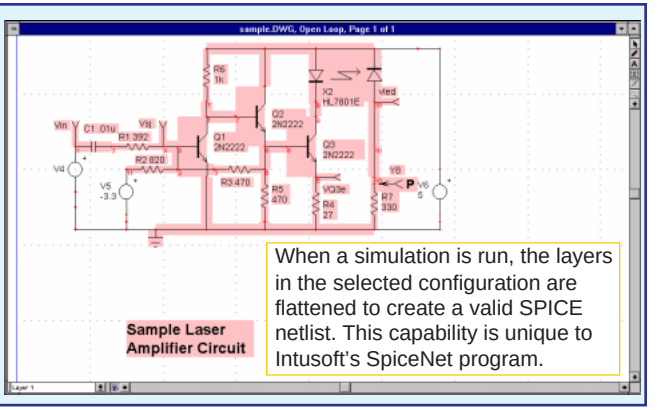


Figure 2, Open Loop circuit configuration. The core circuitry on layer 1 is highlighted and also used in Figure 1. The test circuitry, used here, is on layer 2.

open loop case, we will record the 3dB frequency at the output. You can assign any number of measurements to each test.

Here is the truly revolutionary part. Using the Simulation Control dialog (Figure 3) you can select any number of tests to run automatically. Upon clicking the Simulate Selections button, Design Validator simulates the tests and records all of the measurements. When it's finished, the results are organized into a report containing the measured (simulated) results and the pass/fail grades. The min/max tolerances are used to grade the performance. An example is shown in Figure 4. Note that all described operations are graphically driven.

With the push of a button, Design Validator™ runs all of the simulations and processes the results WITHOUT the need for any user interaction!

The measurement tolerances are assigned automatically, based on data taken in a nominal run. Different pass/fail

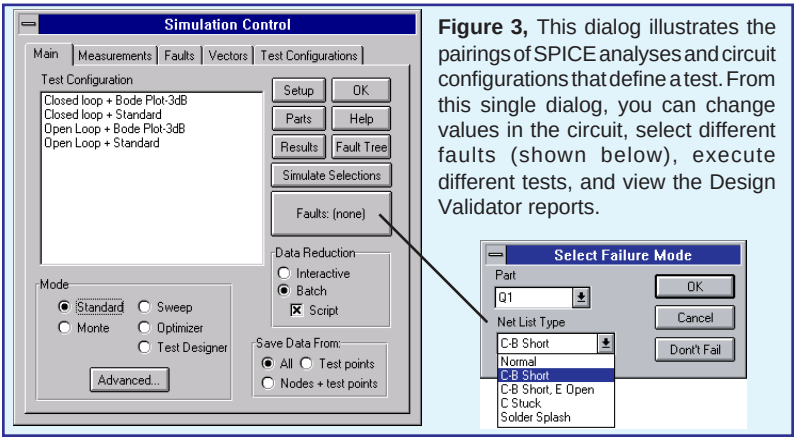


Figure 3, This dialog illustrates the pairings of SPICE analyses and circuit configurations that define a test. From this single dialog, you can change values in the circuit, select different faults (shown below), execute different tests, and view the Design Validator reports.

Table 1 - Design Validator™ Keyword Definitions

What's A Schematic Layer? - A single slice of a schematic drawing. Any portion of a design, or an entire design, can be placed on any layer.

What's A Circuit Configuration? - A set of ***layers*** which are combined and flattened to define a unique circuit design.

What's A Simulation Setup? - One or more SPICE analyses (AC, Tran, etc.) which are grouped together and run at the same time.

What's A Test? - A ***Circuit Configuration*** combined with a ***Simulation Setup***

What's A Measurement? - Scalar value recorded from one or more simulation waveforms (i.e. Maximum, RMS, rise time, etc.) during a ***Test***

What's A Fault? - A hard fault (short, open, or stuck node) or any out-of-tolerance condition (value and/or model parameter deviation)

tolerance limits can be easily assigned, but defaults are inserted for you.

Design Validator™ enables any part of your system to be tested and verified under any condition, including out-of-spec performance variations based on any design change. Design Validator™ is a vast improvement over manual analysis, especially when repetitive comparisons must be made, and dramatically reduces the time-consuming evaluation of large volumes of data.

New ICAP/4 Failure Analysis Features

A new Failure Analysis feature is included in ICAP/4 v8.0. But it really becomes useful when coupled with Design Validator. Normally, you can select any part in the design and choose from a list of hard or soft (out-of-tolerance) failure modes. Then after a simulation, you can analyze the effect of the fault.

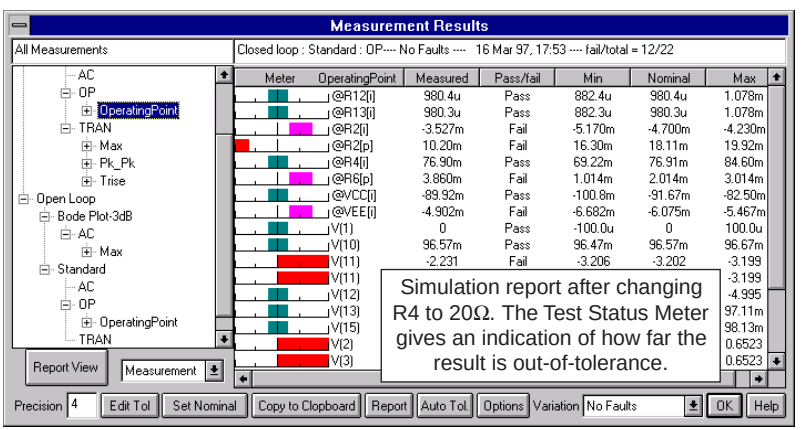


Figure 4, The Design Validator report shows the test results and indicates which tests passed or failed. The measurement tree is shown on the left. The report allows you to easily compare the results of two simulations.

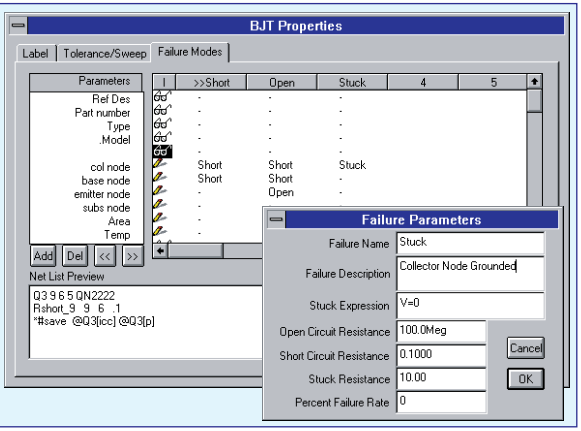


Figure 5, A flexible failure mode definition dialog is included in SpiceNet. You can define and easily select between predefined (CASS standard) and user-defined hard faults or out-of-tolerance conditions. NO script writing, programming, or ideal switch insertion is needed to define a fault. Fault entry is dialog driven.

A list of predefined failure modes is included, but you can easily add your own failure modes as shown in Figure 5.

For model failure mechanisms, ICAP/4 automatically makes a revised .MODEL statement for you without changing the appearance or connectivity of the schematic. There's no need to edit any SPICE subcircuits or to insert switches, resistive opens, etc. in the schematic.

When failure analysis is combined with Design Validator, you get a powerful way to analyze and document the effects of different circuit faults. For example, using the Faults button shown in the Simulation Control dialog, we can open resistor R4 (Figure 3). With a click of the Simulate Selections button, the effects of this change are automatically reported as shown in Figure 6.

Failure Analysis

- Simulate failures, out-of-tolerance conditions, or other user-defined part behavior ("what-if" scenarios)
- Quickly select any defined fault for any component and run a simulation
- When linked with Design Validator™, you can generate reports for any defined fault.

Fault Mode Definition

- Define open, short, and stuck circuit resistance values
- User-defined faults can include expressions of time and other circuit parameters
- All SPICE attributes can be faulted or set out-of-tolerance

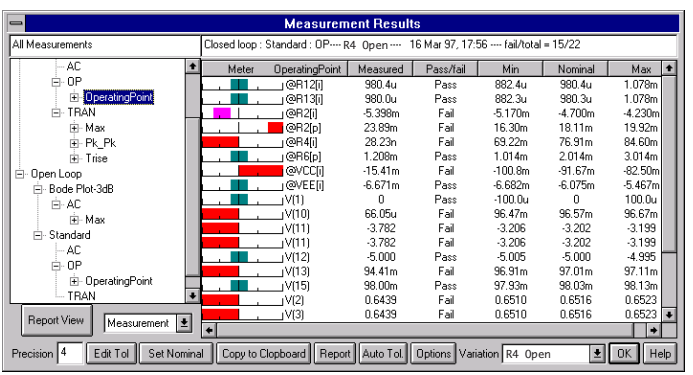


Figure 6, Example circuit from Figure 1 with R4 open. Note how the pass/fail indicator has changed from Figure 4.

INTUSOFT RELEASES NEW SCHEMATIC FREE

Continued from page 1

tures have been added, including several that are not available in any other schematic package.

- Custom SPICE “fill in the blank” dialogs eliminate the need to know SPICE syntax
- All part information (Monte Carlo, Fault, SPICE, packaging) is stored in one design database
- Easily place any of the 10,000+ parts using the hierarchical Parts Browser; no need to preselect symbols libraries
- On-the-fly model/subcircuit editing including model cloning
- Concurrent multiple page, multiple schematic editing
- Embed OLE objects like MS Word equations and Excel graphs
- Unlimited Undo/Redo helps you avoid costly mistakes
- Split screen editing (multiple views of the same schematic)
- Multiple layers/circuit configurations in the same design
- New and enhanced test point symbols (power dissipation, device current, voltage difference)
- Easy-to-use SPICE analysis and stimulus setup dialogs alleviate the steep SPICE learning curve
- Convergence and Analysis Wizards solve problems for you
- Special Part sweeping/Curve family generator allows you to generate a parametric sweep right from the schematic
- Advanced symbol editor uses meta-files and Bitmaps

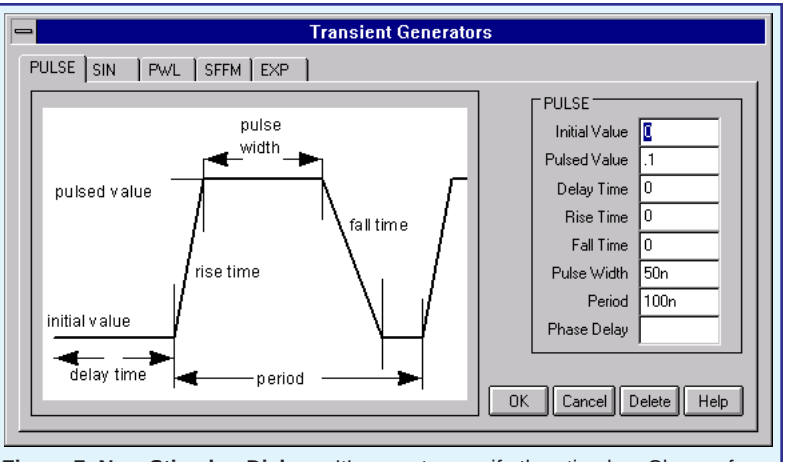


Figure 7, New Stimulus Dialogs, It’s easy to specify the stimulus. Choose from predefined generators (like 3 Phase, PSK, FSK, or NTSC) or define your own with the easy-to-use dialog driven interface.

What's FREE And What Do You Pay For?

ICAP/4Windows version 8.1 includes the new version of SpiceNet and is **available immediately.** An upgrade to version 8.1 from any previous 7.5x version is availabe. Software maintenance is available to accompany version 8.1. Contact Intusoft or your local dealer for pricing. If you have purchased ICAP/4Windows after 1/1/97 the upgrade to version 8.1 is free. A free version of SpiceNet (called version 8.0) can be downloaded from the Intusoft Web Site at www.intusoft.com or the European mirror site at www.softsim.com.

ICAP/4 version 8.1 includes (paid update or new purchase only)**:**

- New SpiceNet schematic entry program
- New ICAPS Program Selector with multiple circuit simulation, Quick Part Edit, and Quick Fault Select features
- Enhanced parametric sweeping and cross-probing
- Enhanced SPICE model libraries (Now with over 10,000 parts when you get the Deluxe version)
- Improved Monte Carlo/Optimization analyses
- Basic analog and mixed signal Failure Analysis capability
- Ability to add the new Design Validator™ and Test Designer™ options

If you download the Free version of SpiceNet from the Web: You get the new SpiceNet schematic entry program with all of its ease-of-use features, wizards, symbol editor, and new interface. SpiceNet will hook into your existing ICAPS system and work with your existing model libraries, and IsSpice4 and IntuScope programs.

Important Note: The existing waveform cross-probing, Alter, and operating point display features in the SpiceNet included in ICAP/4 v7.6 will NOT be available when used with the free version of SpiceNet (v8.0).

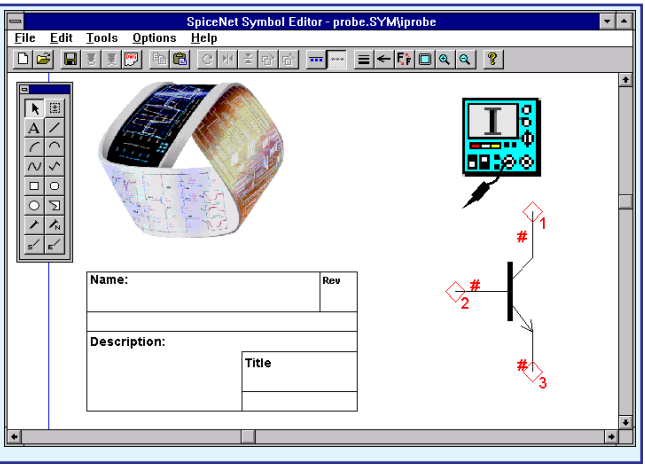


Figure 8, SpiceNet includes a new interactive Symbol Editor. You can import existing symbols and mix them with Bitmap images and Windows .WMF meta-files.

INTUSOFT ADDS SOI MOS MODEL

by B. Iniguez

A new continuous fully-depleted SOI MOSFET model has been implemented in IsSpice4 using the XSPICE-based Code Model Software Development Kit (CMSDK) [1]. This model was developed by B. Iniguez [2, 3] and is the first semiconductor model ever written in the XSPICE analog HDL (Hardware Description Language), also called XDL. The model is charge conserving and presents an infinite order of continuity for all of the small and large signal parameters; a very desirable property. The new SOI MOSFET model is included in the latest version of the ICAP/4Windows (version 8.0) package.

The new model is of great utility for analog design, where continuous and accurate derivatives of the drain current, charges, and capacitances are required. In particular, the model is well-suited for low-power low-voltage analog circuits where charge conservation is critical (like switched-capacitor and current circuits).

Code modeling is the process of creating new SPICE elements using XDL (eXtended Description Language); a C language-based AHDL. XDL models are separate from the simulator. The CMSDK had been used in the past to implement models for system, digital, sampled-data, and behavioral circuit elements.

After the model code is compiled using Microsoft Visual C++, a code model library (DLL) is created, and can be accessed by IsSpice4. Model debugging takes place in the Visual C++ environment using a supplied debug version of IsSpice4. This allows breakpoints to be set and the model performance to be thoroughly reviewed.

SIMULATION RESULTS

The model's accuracy has been checked by simulation of several benchmark circuits. We have not yet been able to do a quantitative comparison of the results obtained with measurements, but the qualitative agreement is very good. In any case, we have obtained excellent agreement with measurements of the modeled channel current, conductances and capacitances of a single transistor.

Since this is the first XDL implemented SOI MOSFET model, we have not compared the simulation results with those provided by another model for the same device. However, we have demonstrated the advantages of infinite continuity and charge conservation, which are inherent to the model, by

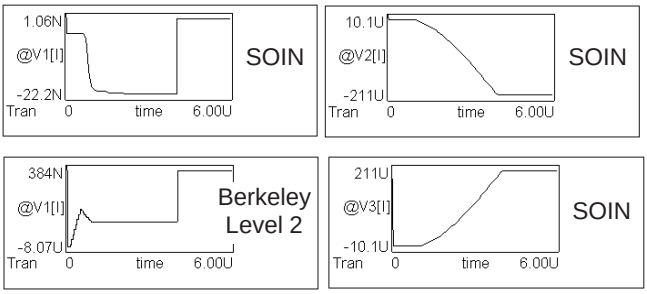


Figure 9, Turn-on of the SOI model as compared to SPICE Level 2. V1[I]=gate current, V2[I]=drain current, V3[I]=source current.

comparison with bulk MOSFET models implemented in Berkeley SPICE.

Fig. 9 shows simulation results for a turn-on transient of a FD SOI nMOSFET using the new model. Because of the infinite continuity of the modeled capacitances, the simulated transient characteristics are continuous from weak to strong inversion. In contrast, simulation of a turn-on transient of a bulk nMOSFET using a Level 2 model can give oscillating gate current values because of the discontinuities of capacitances.

Figures 10 and 11 show the DC and transient response of a SOI CMOS inverter string. The results are qualitatively correct. Note that in SOI CMOS technology, the back gate is common to both n- and p-type devices.

Figure 18 shows the transient response of a transmission gate when it is on, that is where A2 and A4 are on and allow the signal provided by the output of the inverter (A1 and A3) to pass through the gate. Figure 19 shows the simulated output voltage

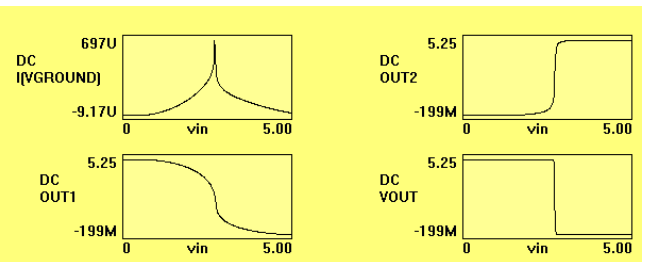


Figure 10, DC analysis of a 3 stage inverter chain. Out is the last stage.

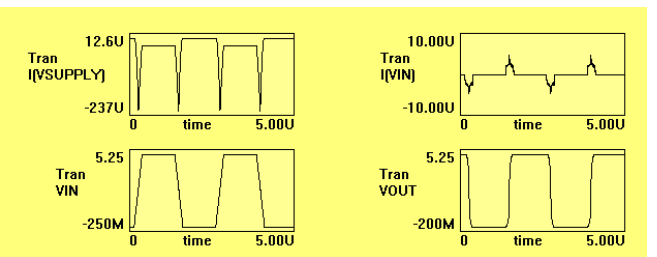


Figure 11, Transient analysis of a single inverter stage. Vin is the gate.

Continued on page 22

MODELING A RELAY

by Mike Penberth, Technology Sources, U.K.

In this article we'll look at how IsSpice4 can be used to model a relay in detail. Figure 12 shows the full model which is split into the following parts:

The Coil and Drive

The transistor drives the coil which is represented by the components between the collector and supply, V3. We might usually think in terms of using a voltage source in the coil circuit to develop the back emf, but this implies differentiating the flux in the magnetic circuit. In this model, we integrate the voltage across the coil (less the resistive drop) to obtain the flux at node 7. When performing a simulation, integration is always preferable to differentiation, and the LAPLACE function provides a very fast and simple integrator.

The Magnetic Circuit & Force

The reluctance of the magnetic circuit has two series components, that of the fixed iron and air path and that of the changing solenoid air gap. For simplicity, we initially assume no fringing and a linear relation between gap and reluctance. Flux flows through the series combination of the reluctances to give a "potential" which is the ampere-turns, V(17). From the ampere-turns we have the current flow in the coil from nodes 1 to 12.

The magnetic force on a body is the integral of the square of the normal component of B over the surface. For a simple solenoid plunger with little fringing, we initially assume B squared times the plunger face area. This, in turn, is the square of the flux divided by the area.

The Moving Air Gap

The plunger acceleration is the result of the sum of the forces which are acting upon it. The acceleration can be double integrated to obtain position with respect to time. The other forces acting on the plunger are friction and the hard stop. Friction is calculated from velocity via a high gain limiter; this gives a constant force whose sign is dependent upon the direction of movement, i.e. static friction. The characteristic of the stop is obtained from a table model which gives a high spring rate for negative gap. The gap position, V(14), is fed back into the magnetic circuit to control the air gap reluctance.

Arcing

The solenoid plunger is connected to the relay contacts. The contact gap closes before the plunger hits the end stop. A limiter

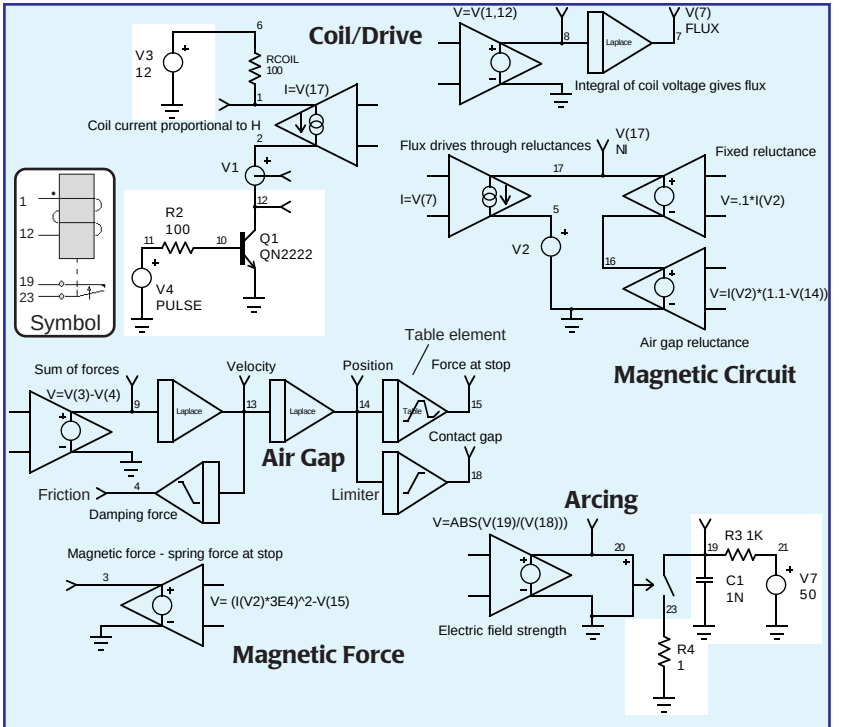


Figure 12, IsSpice4 model of a relay. The model includes the effects of coil impedance, back emf, nonlinear air gap-reluctance relationship, plunger position, plunger friction, plunger stop elasticity, and arcing. Test circuitry is shown in white.

function is used to generate the contact gap from the plunger position. Arcing will occur when the electric field strength across the gap exceeds a certain value. By calculating the field strength and applying it to a switch at node 20, we can short the relay contacts to simulate arcing.

Results

The plot of Figure 13 shows the plunger bouncing off the end stop following coil energization and the rise of current in the coil. Figure 14 shows some detail of arcing at the contacts, node 19, and the contact gap, node 18. An example IsSpice4 netlist is shown in Table 2.

Comments

The constants in this example are purely arbitrary and do not represent any real device. When modelling a real device, it would be relatively easy to introduce some second order effects such as non-linear reluctance change with air gap by using either the equation facilities in the B source, or the table model to introduce data obtained from a field modelling package.

As the air gap widens, fringing increases and the effective magnetic path length becomes longer than the gap. This can be introduced as a second order term in the B source, or added as a nonlinear behavioral resistor.

```
Rgap 16 0 R=(1.1-V(14))+(1.1-V(14))^2
```

As presented previously, the stop is perfectly elastic, energy loss in the stop can be added by subtracting another force computed from the stop force times plunger velocity. For example by changing B10 to read:

```
V=V(3) - V(4) - V(13) * V(15) * .0001
```

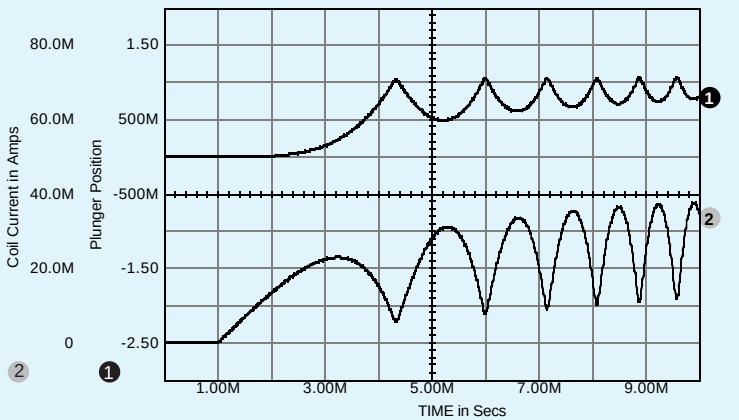


Figure 13, The plunger bouncing off the end stop can clearly be seen from this graph of the plunger position and the energizing coil current.

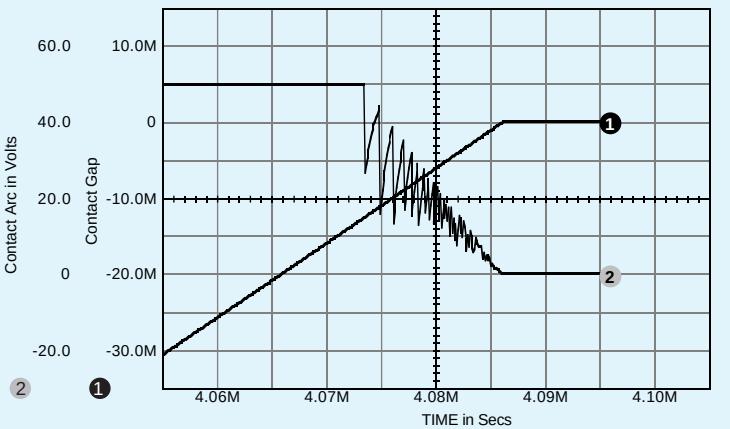


Figure 14, The relay model includes the effects of arcing as shown by this plot of the relay contact voltage as the contact gap is closed.

```
.SUBCKT RELAY 1  12  19 23
*Connections      Crtl+ Crtl-  Out+ Out-
V1 2 12
S1 19 23 20 0 SW1
.MODEL SW1 SW RON=10M ROFF=10G
+ VT=3K VH=1K
B13 20 0 V=ABS(V(19) / (V(18)))
B5 8 0 V=V(1) - V(12)
A1 8 7 S_001
.MODEL S_001 s_xfer(in_offset=0 gain=1.0
+ num_coeff=[1.0] den_coeff=[1.0  0]
+ denorm_freq=1.0)
A2 9 13 S_002
.MODEL S_002 s_xfer(in_offset=0 gain=1.0
+ num_coeff=[1.0] den_coeff=[1.0  0] out_ic=0
+ denorm_freq=1.0)
A3 13 14 S_003
.MODEL S_003 s_xfer(in_offset=0 gain=1.0
+ num_coeff=[1.0] den_coeff=[1.0  0] out_ic=0
+ denorm_freq=1.0)
A4 14 15 PWL_001
.MODEL PWL_001 Pwl(xy_array=[0  0  1.0
+  0  1.1  100.0Meg  1.2   200.0Meg]
+ input_domain=10.0M fraction=TRUE)
A5 13 4 LIM_002
.MODEL LIM_002 Limit(in_offset=0 gain=1K
+ out_lower_limit=-10 out_upper_limit=10
+ limit_range=1.0U fraction=FALSE)
A6 14 18 LIM_001
.MODEL LIM_001 Limit(in_offset=-0.8
+ gain=1 out_lower_limit=-10K
+ out_upper_limit=-1U limit_range=1U)
B7 1 2 I=V(17)
B8 17 5 I=V(7)
V2 5 0
B12 17 16 V=.1 * I(V2)
B4 16 0 V=I(V2) * (ABS(1.1-V(14)) +
+ (1.1-V(14)) * .5  ; Use Rgap for
* nonlinear air gap effects
* Rgap 16 0 R=(1.1-V(14))+(1.1-V(14))^2
B10 9 0 V=V(3) - V(4) -
+ V(13)*V(15)*0.0005   ; added for
* Imperfect plunger stop
B11 3 0 V=(I(V2) * 3E4)^2 - V(15)
* 3E4 Plunger area
.ENDS
```

Table 2, IsSpice4 relay netlist.

Relay Model Comparison

Many analog simulation tool vendors claim to have a large number of SPICE models in their libraries. But when you look more deeply into their offerings, you will see that there are significant shortcomings for which numbers of parts are not a substitute.

Take, for example, the relay we just reviewed. The relay models found in Electronic Workbench and CircuitMaker are shown in Figure 15. The relays use only the ideal SPICE (two-state) switch to model the relay. No nonlinear inductive, mechanical or arcing effects are included in their models.

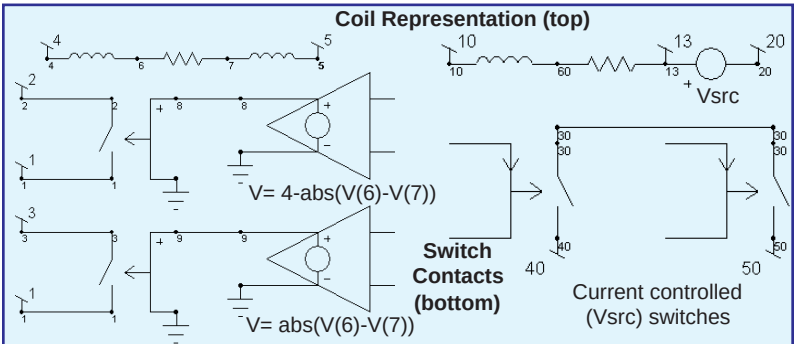


Figure 15, The relay models from CircuitMaker (left) and Electronic Workbench (right) don't include key features found in the real devices. The models are first order and support only coil inductance, turn-on current, holding current, and coil resistance.

By comparison, the models in these products are simplistic and only model "first order" phenomenon. First order models have their place in the simulation process. They are quite useful, especially for system level simulations, and Intusoft includes them in ICAP/4.

However, while these software products can be less expensive, you will find that you really get what you pay for when it comes to model features and performance. Good models are CRITICAL to a successful simulation, and they don't come cheap. The quality of a model library should not be judged by how many models are included, but by the effects that the models emulate. The number of models simply doesn't tell the whole story.

For further information on this article, contact Mike Penberth at: **Technology Sources Ltd. U.K. Tel: +44-01 223 516 469, Fax: +44-01 223 729916, Web - www.softsim.com.**

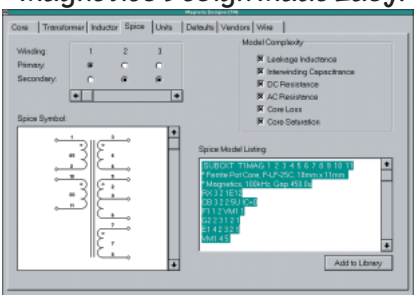
NEW SMPS BOOK AVAILABLE

Intusoft is pleased to announce the availability of an important NEW SPICE reference book. The book, entitled *SMPS SIMULATION WITH SPICE3,* is published by McGraw-Hill. It is authored by Steve Sandler, a well known authority in the power electronics and simulation arena. The book is a **MUST HAVE for every power circuit designer** who is using or thinking of using SPICE. It includes information on magnetics and power supply modeling, simulation, and circuit design techniques. There is also a chapter from renowned magnetics expert Rudy Severns on **Modeling Magnetics** (inductors, transformers, nonlinear core models, and reluctance modeling). Topics in the new book include:

- **EMI Filter Design:** Using SPICE to calculate harmonic content
- **Buck-Flyback Topology Converters:** Average vs. Transient Modeling for Voltage/Current Mode control
- **Linear Regulators:** Control Loop Stability
- **DC-AC Conversions:** State machine modeling, Sine ROMs
- **Improving Simulation Speed:** Tips for Power Supply Designers

The book is specially priced and is available from Intusoft or your local Intusoft dealer immediately.

NEW MAGNETICS DESIGNER UPDATE



Intusoft has updated its popular transformer and inductor design program, Magnetics Designer. The new version contains a greatly expanded core database with thousands of new cores and several new materials. The new materials include W and H from Magnetics and PC44 from TDK, to name a few. A partial list of the new core geometries includes Toroid, EP, RS, and DS ferrites from Magnetics, and EPC, LP, and EER ferrites from TDK. Other features include the ability for the user to define winding-related calculations like current density, power, losses, thickness, and winding pitch.

Magnetics Designer synthesizes and analyzes various types of transformers, inductors, and chokes. Typical designs may include ferrite pot, EE, EP, cut C, planar and RM cores, toroids, and EI laminated cores. Typical applications include 60 Hz line transformers, switching regulator transformers, and output filter inductors. The program produces electrical and winding reports and a SPICE model along with the finished design.

For more information, see the Intusoft Web site. Contact Intusoft or your local dealer for prices. The update is free for registered customers who purchased after 1/1/97, otherwise there is a charge. More information and a demo version of Magnetics Designer is available on Intusoft's Web Site.

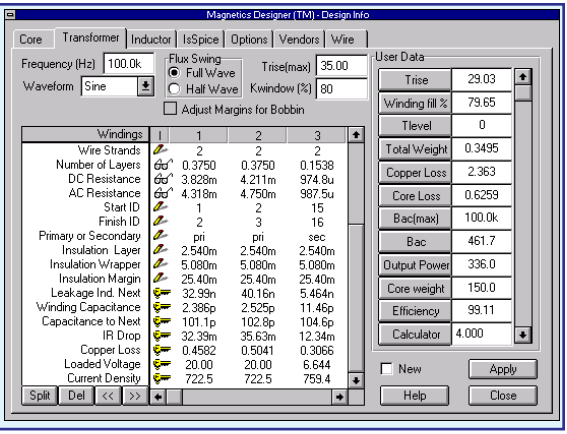


Figure 16, The new Magnetics Designer program allows you to enter your own winding related equations. Shown bottom left are the new calculations of IR drop, copper loss, loaded voltage, and current density.

ELIMINATING CONVERGENCE PROBLEMS

Convergence problems come in all shapes, sizes, and disguises. They are normally caused by incorrect circuit topologies, unrealistic device modeling, or improper model usage. Circuit topology problems are usually related to "operator" errors. For example, circuit connectivity errors or SPICE syntax mistakes like using the letter "O" instead of the number zero, or using M for 1E6 instead of MEG. Device model-related problems can be difficult to solve, especially if they are related to the model's characteristics and capabilities. Fortunately, Intusoft's models are carefully tested and modeling issues tend to be related to using the model for a purpose for which it was not intended.

There are many instances, however, where SPICE can diverge from the correct answer due to numerical instabilities or the idealized nature of a device's representation. In these cases, simply adjusting SPICE's internal defaults (.Options param-

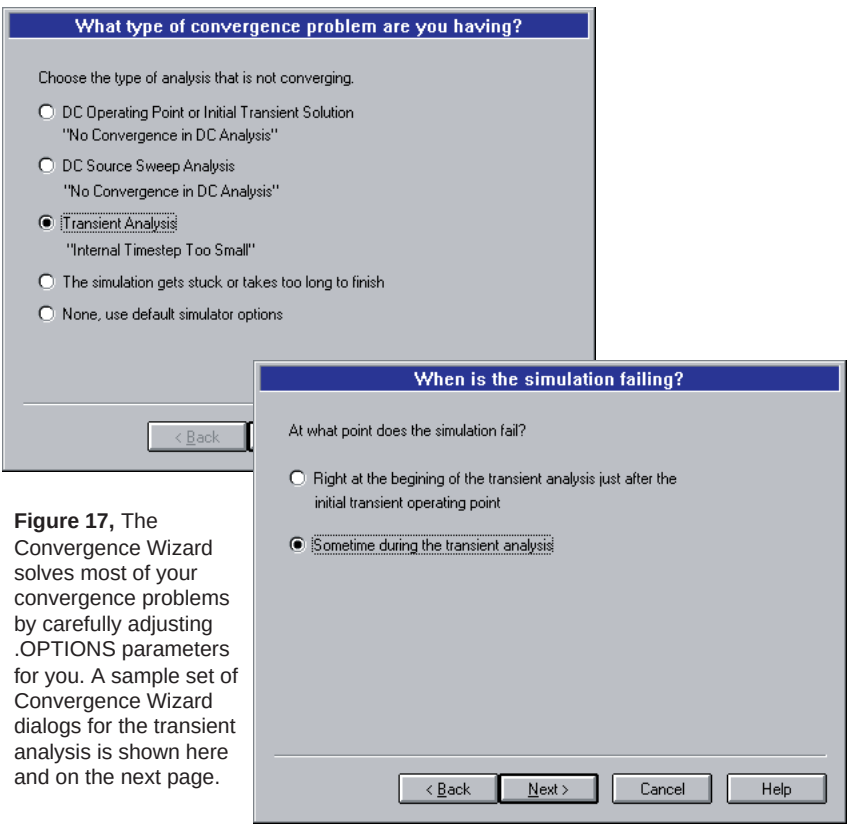
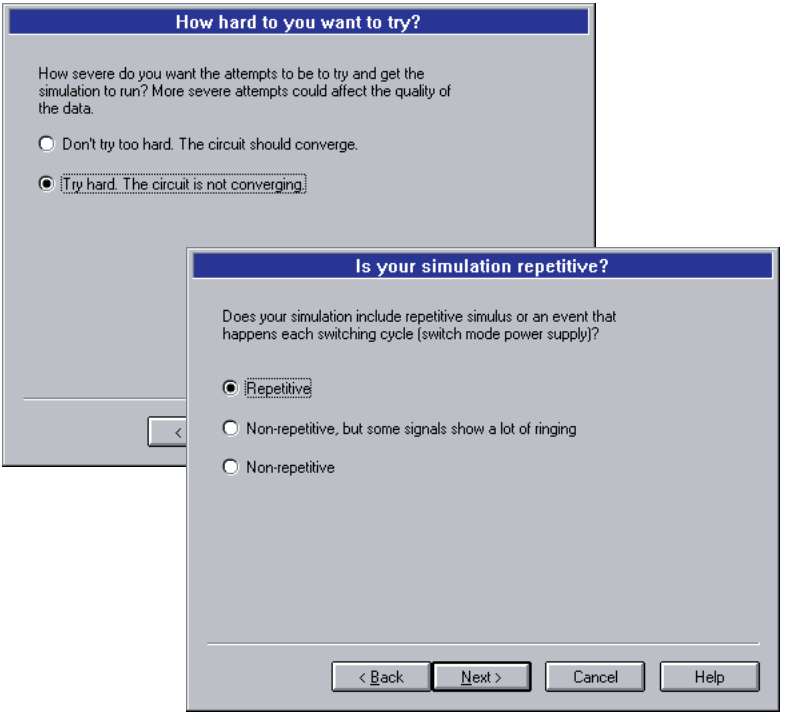


Figure 17, The Convergence Wizard solves most of your convergence problems by carefully adjusting .OPTIONS parameters for you. A sample set of Convergence Wizard dialogs for the transient analysis is shown here and on the next page.



eters) can VERY often be sufficient to solve the problem. In fact, .Options values have a far greater effect on simulation results than various algorithmic differences you might find among different SPICE vendors. Thus, claims of one SPICE vendor's superior convergence over another are dubious at best.

The key hurdle is knowing which .OPTIONS parameters to change and what values to enter. This is where the new **Convergence Wizard** feature comes to the rescue. The Convergence Wizard guides you through a series of simple questions (Figure 17). Based on your answers, it adjusts the .Options parameters for you. The result is that you no longer have to remember the SPICE syntax and most of your toughest convergence problems are solved for you automatically.

The new ICAP/4 v8.x, as well as the ICAP for OrCAD, Protel, and Viewlogic systems include the Convergence Wizard. It's like having a SPICE guru right in your computer!! For detailed information on how the Convergence Wizard works, please see the reference below or try it yourself using the free SpiceNet program posted on the Intusoft web site.

[1] "Step-by-Step procedures help you solve Spice convergence problems", Charles Hymowitz, EDN Magazine March 3, 1994

WHY IsSpice4 IS BETTER!!!

IsSpice4 provides a quantum leap in performance over other analog and mixed mode simulators. It is the first commercially available version of SPICE based on Berkeley SPICE 3F and Georgia Institute of Technology's XSPICE.

IsSpice4 allows you to explore circuit performance by interactively running different analyses and sweeping any circuit variable. With the ability to simulate electrical, sampled-data, mechanical, physical, thermal, and other systems, **IsSpice4 is the ONLY true native mixed mode SPICE 3 based simulator.** The advanced features of IsSpice4 allow all types of applications to be simulated: switch mode power supplies, mixed signal ASICs, RF communication systems, interconnects, control systems, and mixed mechanical/physical systems.

Intusoft has spent hundreds of man-hours improving SPICE. And although IsSpice4 is based on SPICE 3, Intusoft has greatly enhanced the program over and above the public domain version and added more features, an interactive interface, superior analysis and model support, and improved convergence algorithms - all for a price no one can match. IsSpice4 is simply the best and most affordable SPICE program on the market today. Just take a look at some of its features:

State-of-the-Art Operation

- Native mixed mode simulation - IsSpice4 includes an event driven simulator that supports mixed analog, digital and DSP circuits.
- Interactive Operation - IsSpice4 operates interactively, and frees you from the restrictive batch style of older SPICE simulators.
- Interactive Command Language - Comprehensive set of functions for batch style control of the simulator
- ***NEW VISUAL BASIC SCRIPTING*** - Drive IsSpice4 using VB scripts from popular programs like Excel.
- ***NEW OLE INTERFACE*** - Develop your own OLE interfaces or connect user-defined algorithms to IsSpice4

Built-in Models

- Elements: Resistors, Capacitors, Inductors, Coupled Inductors, Transmission Lines, Diodes, BJTs, JFETs, MOSFETs (Level 1-8), GaAs Mesfets, Switches, and Boolean logic expressions.
- Digital and AHDL Models: Digital primitives, State Machine, Frequency Divider, RAM, Sampled-Data Filters, Nonlinear VCOs, Laplace Equations
- Behavioral Modeling: In-line Equations, Table models, If-Then-Else

Advanced Models

- HDL Models and C Subroutines; Create models based on a powerful nonproprietary HDL using C
- Support for nonelectrical applications and top-down system design
- Three types of digital/mixed mode modeling
- Lossy (distributed) transmission lines with frequency dependent losses
- MOS: BSIM1, BSIM2, and New BSIM3 version 3 and SOI MOSFET models

Analysis Support

- AC, DC, transient, noise, Fourier, distortion, DC/AC sensitivity, Pole-Zero analyses, and Temperature variations on individual elements
- Monte Carlo Analysis, Circuit Optimization/Performance Analysis
- ***NEW DESIGN VALIDATOR***™ for automatic design verification
- ***NEW TEST DESIGNER***™ Fault Analysis and Software Test Set Design

Additional Interactive, AHDL & Mixed Mode Features

- Real-time Display of voltages, currents and power dissipation
- Simulation Scripts: a robust scripting language that allows simulation breakpoints and loops of different analyses to be run as a test procedure.
- Interactively run analyses without having to edit the netlist or restart the simulator, add, delete, or rescale waveforms on the real-time display
- Digital Simulation: IsSpice4 includes a 12 state digital logic simulator and models with timing information
- Sweep parameters one at a time or in groups with great ease
- Start, stop, pause, change, or resume any analysis on demand
- Use C code subroutines & AHDL models based on XSPICE

Convergence and Speed Improvements

- Automatic Gmin stepping/Source stepping algorithms
- New Pseudo-Transient algorithm
- Improved Predictor-Corrector, Latency, and Bypass algorithms
- Improved program defaults
- Special Circuit Debugging Options
- Full Gear Integration option

Compatibility

- True OLE Integration with popular schematic entry programs

DID YOU KNOW INTUSOFT WAS THE FIRST?

The following is a list of capabilities that Intusoft introduced to the analog simulation world.

- **SPICE 2 Models for:** IGBTs, fuses, lasers, vacuum tubes, generic template models, dual gate Mosfets, SC filters, neural networks, digital gates, RF beads, IBIS buffers, saturable cores, and PWMs (using the state space approach)
- **Products/Features:** 32-bit version of SPICE for DOS, integrated schematic entry dedicated to SPICE, SPICE 2 compatible model generation software, support for all Macintosh platforms, parameter passing

A SPICE FOR EVERYONE!

Affordability is the hallmark of Intusoft's products. With our new ICAP/4Rx, ICAP/4Windows, and ICAP/4Macintosh software, all affordably priced, there's an IsSpice that's just right for you.

New ICAP/4Rx

YOUR PRESCRIPTION FOR REDUCED COMPLEXITY

If you've been looking to upgrade your evaluation version of SPICE, or are thinking about getting started with SPICE, we'd like to suggest a system that's easy to learn but powerful enough to tackle all of your design jobs. It's called **ICAP/4Rx** and it's a complete circuit simulation system that includes everything you need to simulate all types of system, board, and IC level circuit designs.

The ICAP/4Rx system strikes a perfect balance between ease-of-use and power. It has the power to handle tough designs, and removes the steep learning curve associated with using SPICE. And it does this without compromising power as some other electronic workbench systems do, and at a reasonable cost (unlike Microsim's™ Pspice®).

Simulation Environment

- Full SpiceNet Schematic Entry and IntuScope waveform analysis tools
- Unlimited circuit size allows you to simulate large designs
- State-of-the-art SPICE 3 and XSPICE-based simulator with all SPICE 2 and SPICE 3F elements
- All major SPICE analyses: AC, DC, Operating Point, Transient, Fourier, Temperature and Parametric "What-If " analyses
- Limited Mixed mode simulation (Boolean expressions/transistor gates)
- Interactive analyses and parameter sweeping with ICL Scripts
- Real time waveform display of ALL voltages, currents, & power dissipations

Who is the Real Price Leader?

Intusoft pioneered low cost SPICE over 10 years ago with the introduction of IsSpice at the unheard of price of $95. Our competitor was charging **10 times the price** for comparable capabilities. With ICAP/4Rx, we continue to lead the way with the **least expensive entry solution** that performs the capabilities you need most. ICAP/4Rx is your prescription for reduced complexity.

SPICE Features

- Comprehensive SPICE Model Library (3000 parts)*
- Powerful and PROVEN IsSpice4 simulator
- Advanced Behavioral Modeling: Math expressions, If-Then-Else, Table & Laplace models
- AHDL Models, BSIM3 version 3
- Advanced SPICE 3F.5 Convergence Algorithms
- Includes All vendor supplied IC models

*See the Intusoft Web Site for a complete listing.

WHY IS ICAP/4Rx SO EASY-TO-USE?

ICAP/4Rx is an integrated circuit simulation system including our 5th generation schematic entry tool, proven IsSpice4 simulator, waveform post processor, and SPICE model libraries. It is reduced in complexity in order to provide you with the easiest simulation environment to use.

ICAP/4Rx goes on sale May 1, 1997 until 7/31/97.

After 7/31/97 ICAP/4Rx will be go up.

New Graphical User Interface

- Easy-to-Use Integrated Schematic-SPICE environment
- No need to learn SPICE syntax, all functions graphically driven
- Advanced Waveform Cross-probing; Waveforms can be shown directly on the schematic or in IntuScope with a single mouse click
- New “Parametric Sweep” tool painlessly generates curve families
- Integrated Symbol Editor; Uses .BMP and .WMF files
- Custom attribute dialogs for each part; on-the-fly model/subcircuit editing

Wizards

- Analysis Wizard alleviates the need to learn SPICE syntax
- Convergence Wizard solves common simulation problems for you

Other Features

- No Hardware Protection Key
- Compatible with virtually all schematic capture programs

Benefits To New Users

- New schematic interface makes it easy to get results instead of headaches
- Integrated schematic-simulator solution makes you instantly productive
- **No Need To Know SPICE Syntax**
- Our mature 4th generation SPICE 3F program, IsSpice4, is time-tested and gives you accurate answers you can trust
- Graphical waveform analysis with multiple windows and cursor measurements gets the most out of SPICE
- Reduced complexity makes using ICAP/4Rx effortless

Cost Difference Upgrade to ICAP/4Windows

ICAP/4Windows includes a number of key features that are not found in ICAP/4Rx. But as with ALL Intusoft software you can upgrade for the price difference.

Native Mixed Mode simulation
Full ICAP/4 Model Libraries (10,000+ models)
More advanced IsSpice features (Interactive Sweeping, VB/OLE Interfaces)
More advanced IsSpice analyses (noise, distortion, sensitivity)
Monte Carlo analysis
Circuit Optimization
Ability to use Design Validator™ and Test Designer™
Failure Analysis

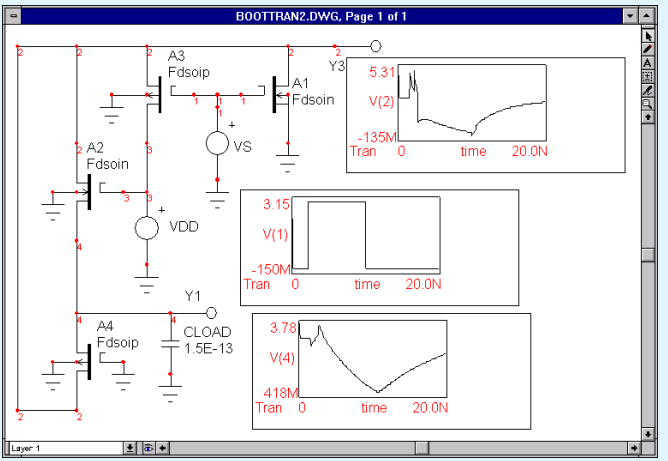


Figure 18, Transmission gate simulation.

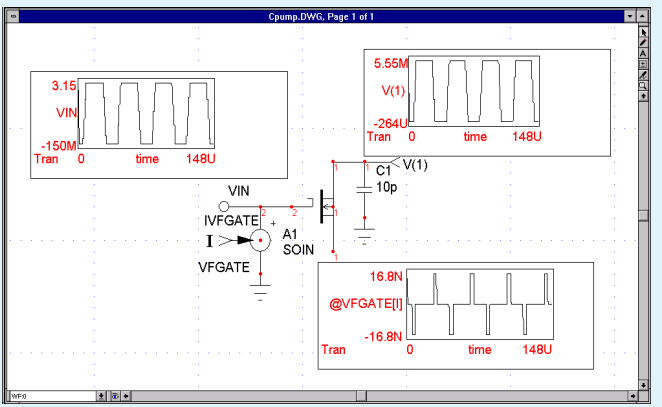


Figure 19, Charge Pump circuit using the SOI Mosfet model.

Continued from page 9

waveform of a charge pump. The waveform is qualitatively correct because of charge conservation. Charge models that are not conservative give erratic outputs.

For the first time, we have implemented a complete transistor model in the IsSpice4 circuit simulator using an AHDL. The charge-based formulation of the model, and its infinite order of continuity for all small and large signal parameters makes the implementation straightforward, and results impressive.

[1] Code Model SDK, ICAP/4, Intusoft, 1994.
[2] UIB, Universitat de les Illes Balears, Spain), and D. Flandre, L. F. Ferreira and B. Gentinne from UCL (Universite Catholique de Louvain, Belgium
[3] B. Iniguez, L. F. Ferreira, B. Gentinne and D. Flandre, “A Physically-Based Continuous Fully-Depleted SOI MOSFET Model for Analog Applications”, IEEE Trans. on ED, vol. 43, no. 4, Apr. 1996.