Intusoft Newsletter

Personal Computer Circuit & System Design Tools

intusoft

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THE SPICEFARM™ IS COMING IN '98

Supercharge your SPICE simulation power with up to 25 Giga-ops of computing power using Intusoft's New **SpiceFarm™**. The SpiceFarm is a bank of 32 interconnected state-of-the-art Pentium II computers optimized to run SPICE. The SpiceFarm can be accessed **securely over the Internet** or locally on your internal TCP/IP LAN. It empowers your SPICE capability by enabling remote

Continued on pg. 19

In This Issue

NEW ICAP/4 V8.x.3

Version 8.x.3 of ICAP/4Windows, the Virtual Circuit Design Lab, includes a number of significant enhancements, including a hierarchical drawing capability with graphical tree navigation, a new Symbol Wizard, ...

Continued on pg. 2

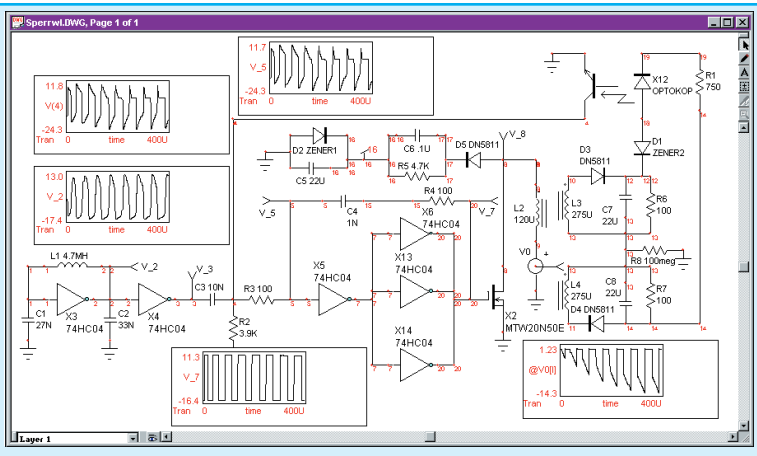

Figure 1, The latest ICAP/4Windows version includes a timesaving autobridging feature that makes interfacing and simulating mixed-signal designs easier.

ICAP/4 V8.x.3 GETS NEW FEATURES

Continued from page 1

Autobridging for automatic analog-digital element interfacing, and user-configurable tool bars. An export netlist feature has been added that outputs Bill Of Materials (BOM), SPICE subcircuits, and various PCB netlist formats. The hierarchical features are accompanied by a unique "Save As SubDrawing" feature (Figure 2) which makes creation and maintenance of subcircuits and design reuse simple and easy.

ICAP/4 - New Features and Benefits

- Hierarchical Design Support including Graphical Tree navigation
- Automatic Subcircuit/Symbol Creation makes hierarchical design entry and reuse simple
- Symbol Wizard for painless creation of symbols
- Export of various netlist formats including PCB, BOM and SPICE subcircuit
- User Configurable Tool Bars
- AutoBridging for simpler Mixed-Signal and Analog-Digital element interfacing
- Support for all types of main and subcircuit parameters, including Pspice® syntax support
- Expanded Model Libraries >13,000

The new ICAP/4Windows system, when coupled with the new Mechatronics library (page 6), adds over 3000 new SPICE models, bringing the total to over 13,000. This represents the largest library in the SPICE simulation industry, with over 400 model types!!

Movies Make Learning SPICE Easy

New Multimedia Movies (that use video and audio to teach SPICE) have been added. The movies cover everything from how to capture a schematic, to how to perform circuit simulations and create new SPICE models. The movies dramatically reduce the learning curve associated with circuit simulation, and make learning the software much easier.

New Intusoft Maintenance Policy

The ICAP/4 version 8.x.3 release marks the first release under the Intusoft Maintenance Program which began in mid-1997. Under this program, updates are supplied only to those customers who have up-to-date maintenance or whose software is currently under warranty (purchased within 30 days of the maintenance release). Intusoft began this program because of the forecast for numerous updates in the near future as the ICAP/4 software

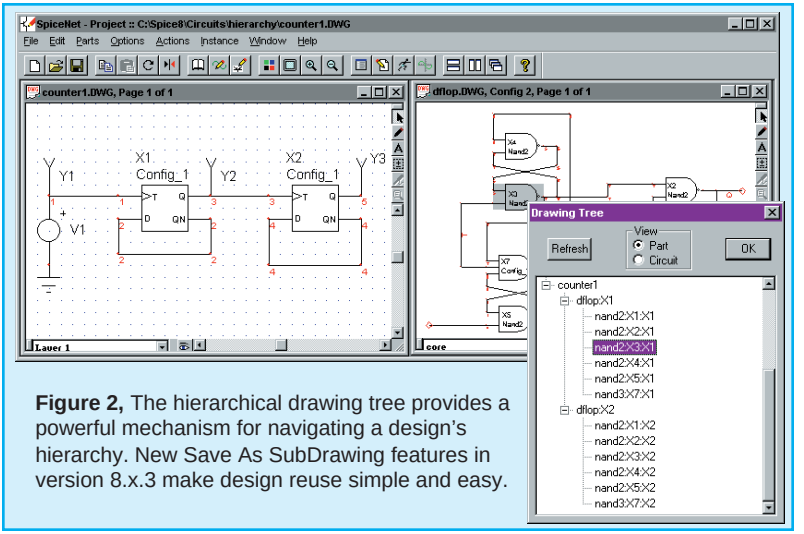

Figure 2, The hierarchical drawing tree provides a powerful mechanism for navigating a design's hierarchy. New Save As SubDrawing features in version 8.x.3 make design reuse simple and easy.

converted to ActiveX technology. We plan several more major maintenance releases in 1998, including a replacement for IntuScope, the SpiceFarm enabled internet-simulation software, and lots of new enhancements for IsSpice4 and SpiceNet.

These upgrades won't be accompanied by price increases; therefore, Intusoft changed its historical approach to selling updates at the price difference to a maintenance based approach.

Along with the 8.x.3 versions, a new copy protection key or "dongle" will be delivered. The new dongle has built-in information that supports de-encryption of files which are placed on the Intusoft web server.

In the near future, you will be able to download models and software updates, and access our SpiceFarm simulation server using the new dongle. You won't have to wait for delivery of the maintenance CD to get the latest features.

If you have not purchased maintenance and wish to get the 8.x.3 update, you will have to bring maintenance up-to-date by purchasing the appropriate maintenance/ upgrades retroactive to the date of your 8.x.1 or 7.x purchase. Maintenance is priced at 15% of the current Intusoft retail price per year. Please contact intusoft of your local intusoft dealer for further pricing information.

CONFIGURABLE SCHEMATICS: A NEW PARADIGM

The ICAP/4 and Test Designer packages feature a unique schematic entry tool with features that greatly ease the test design process and the bookkeeping associated with different hardware test setups.

A key problem for the test engineer is to account for the effects of the test fixture. The design engineer is usually more concerned with the operation of the circuit. This disparity means that the test engineer must modify the schematic to include the effects of IC tester signal generators, the interconnection lines to the DUT(Device Under Test), and the parasitic effects of the test apparatus and probes. The tracking of the test setups related to different test configurations can cause bookkeeping mistakes and waste valuable time debugging working circuitry.

The SpiceNet schematic tool solves this problem by using a "layered" approach to schematic entry. For example, Figure 3 shows a schematic of an IC, referred to as the DUT. It is highlighted and captured on what we will arbitrarily call the DUT layer (note the pop-up in the lower left corner of the schematic). The remaining circuitry (test stimuli and loads) are on separate schematic layers.

In Figure 4, the DUT circuitry is the same, but the test circuitry and stimulus has been changed in order to allow a different test to be performed. The DUT layer is the same for both schematic configurations. Any change made to it will be propagated across the two "schematic configurations". In addition, both configurations are stored in the same design database.

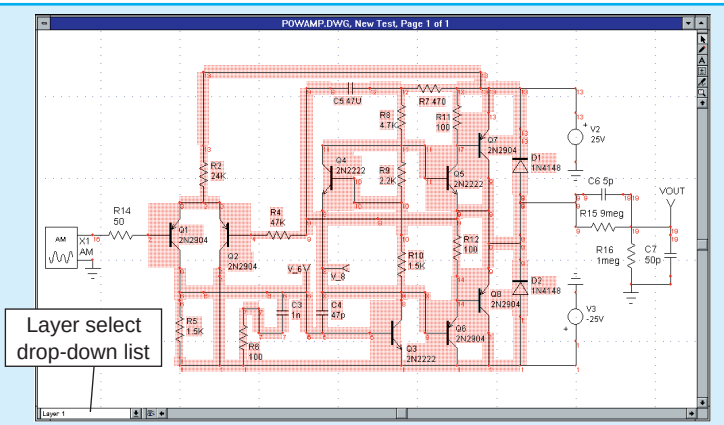

Figure 3, Schematics can be reconfigured using a series of layers. Here we see the DUT (highlighted) on layer 1; the test circuitry is on another layer (layer 2).

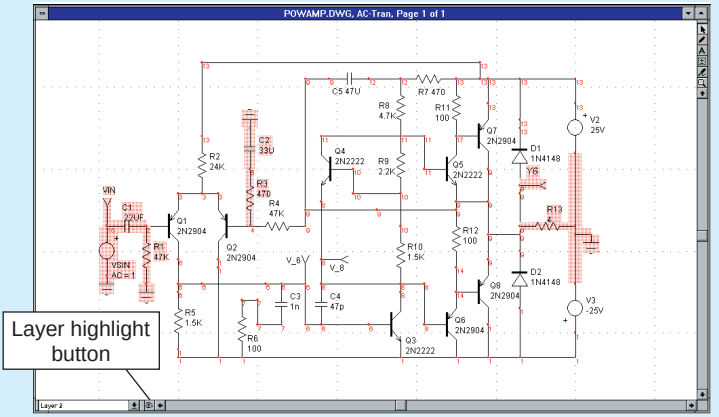

Figure 4, The second circuit configuration consists of the same DUT layer as in figure 2, but a different layer (layer 3, (highlighted)) contains different stimulus.

Unlike other schematic capture programs, the Intusoft configurable schematic tool solves the problem of multiple hardware configurations. The design and test process is better documented, and the design engineer can enhance the core design while the test engineer can simulate the effects of the test fixture, using the results to better set test limits.

ANALOG & MIXED-SIGNAL TEST

Test Designer is a new productivity tool for test engineers who develop and verify test programs and test fixtures for analog, mixed-signal, and mechatronic circuits. It can also act as an extension of the design process, allowing the design engineer to develop test limits and procedures well before the first silicon or prototype breadboard is available.

Test Designer shortens the test development time and allows test development to begin early in the design process, thereby helping to reduce overall time-to-market. Test Designer also improves utilization of expensive Automatic Test Equipment equipment by allowing test development which is independent of the tester.

It provides a structured environment supporting consistent and thorough documentation and a complete methodology from schematic entry through verification and ATE code generation.

Test Designer produces a fault dictionary with diagnostic reports as well as ATE-independent code that describes the test sequence, limits, and resulting ambiguity groups. Test Designer is the FIRST and ONLY tool to bring these technologies together in one complete package. The result is a revolution in analog and mixed signal test with **DRAMATICALLY IMPROVED PRODUCTIVITY.** For more information contact intusoft or check out the our web site.

MECHANICAL MODELS FOR PSPICE® AND ISSPICE4

Intusoft has introduced a new SPICE model library for Mechatronic devices, including models for both **mechanical** and **hydraulic** elements. Key models such as motors, spark gaps, pumps and valves, which are necessary for the successful simulation of automotive and other physical systems, are represented in the library. The new library enables designers to simulate mixed technology circuits which contain both nonelectrical and electrical devices.

Pspice® Users Take Note: The library is compatible with BOTH Pspice and IsSpice4. **That means Pspice users can now perform Mechatronics simulations too!!**

This is the first SPICE library which contains a comprehensive set of models for mechanical, hydraulic, motor and mixed-technology applications. The new library (Figure 6) represents a major breakthrough for mechanical and system designers.

Previous models were based almost exclusively on proprietary HDL models and are almost impossible for the user to view, edit, and understand. With IsSpice4's advanced behavioral modeling capabilities, coding of the new models in an AHDL was unnecessary. Most models in the library are also created with multiple levels of complexity. This allows you to select the appropriate model features of interest and thus control the simulation efficiency.

The library will available January 20, 1997.

Information about the models, including a complete listing of the devices, is available on the Intusoft web site.

Figure 5 shows a typical example of how the models might be used; in this case, in a cascade current-velocity-position control system.

The desired position, Vstep, is compared with the (sampled) feedback signal, FIS, from an encoder, and sent through a Limiting PI-Controller (LPIC). The output, which is the desired voltage, is compared with the return signal, WS, from a tachometer. Then it (Vwd) is sent to a second LPIC, which calculates the desired motor current. The current signal is sent through a limiter (LIMIT), compared with the signal (IS) of a current sensor

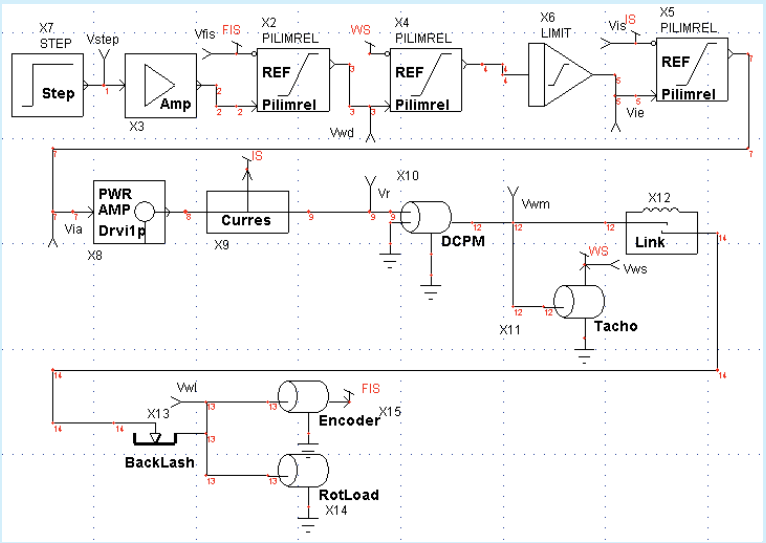

Figure 5 - The schematic of a cascade current-velocity-position motion control system using elements from the new Mechatronics Library.

(Curres) and sent through a third LPIC. The output (Via) of this LPIC is the control signal for the power amplifier, which converts the AC net voltage to a DC voltage. The motor is a permanent magnet motor. A flexible coupling with backlash connects the motor to the rotational load.

The netlist and simulation results for this mechatronic circuit will be shown in the next *Intusoft Newsletter* where we will explore the circuit in greater detail. We will also take a look at how some of the motor models are developed and how mechanical FAULT ANALYSIS can be employed to investigate the circuit's failure behavior.

Figure 6 - Model Types in the New Mechatronics Library

- **Stimulus sources, Drive controllers** (PID, DC/1 phase, 3-phase)
- **Electro-mechanical actuators** (***DC Motors:*** permanent magnet, separately excited, series excited, shunt excited, compound excited, 3-phase brushless, ***AC Motors:*** 3-phase induction, 1-phase induction, 3-phase synchronous, ***Stepper Motors:*** 2-phase permanent magnet, 3-phase permanent magnet, 2-phase variable reluctance, 3-phase variable reluctance, and a 3-phase switched reluctance motor, and solenoid)
- **Electro-hydraulic actuator models** (displacement pump, hydraulic motor)
- **Mechanical models** (gears, flat belt, brake model, clutch model, cam model, pulleys)
- **Sensors** (tachogenerator, encoder, accelerometer, vibrometer)
- **Translational mechanics models**
- **Rotational and mixed rotational/translations mechanics models**
- **Planar mechanical models**
- **Hydraulic models** (pipes, tanks, leaks, loss due to bend, orifice flow, gas loaded accumulator, pressure relief valves, hydraulic power drives)

SPICE SIMULATES A FLUORESCENT LAMP

Christophe BASSO, consultant, SINARD, FRANCE

A Hot Cathode Fluorescent Lamp (HCFL) is a device in which a gaseous mixture flows between two tungsten electrodes or filaments. In domestic applications, the mixture is made of mercury vapor and a small quantity of inert gas (krypton or argon). The role of the inert gas is to vaporize the mercury during the turn-on phase. To lengthen the filament lifetime, a preheating period is necessary in order to bring the electrodes to a sufficient temperature before the tube avalanches to its on state. The warm-up is performed by supplying the filaments with a DC or AC current during the first few hundred milliseconds. During this emissive period, the filaments increase the electron population in the tube, and consequently decrease the avalanche potential resulting in a lower striking voltage for the lamp. Once the lamp is struck, it maintains a quasi-constant voltage across its end points. This value is called the arc voltage. A practical value for the cold striking voltage for a 5 foot lamp (58W) is near the kV range with the corresponding arc voltage around 110Vrms.

An HCFL can be operated at low or high frequencies. At low frequency, e.g. in a 60 or 50Hz ballast application, the conducting gas reacts faster than the AC line. Every time the polarity of the mains changes, the lamp current cancels and the tube halts its conduction process. It then has to restrike with the opposite polarity, but at a voltage lower than its cold value because of the temperature. At this slow operating rate, a second effect can be noticed; due to the negative impedance characteristics of the conducting gas, the voltage across the tube will decrease as the current grows. At higher frequencies, above a few kHz, these effects are smoothed out and we can represent the tube using resistive and weakly capacitive behavior.

The SPICE modeling for a fluorescent tube can be generated in several ways [1]. Fitting the I/V characteristics with a polynomial equation represents an elegant solution, but the parameter extraction from the manufacturer's data curves is invariably a complicated process. In contrast, the SPICE macro-modeling technique offers a simplified and efficient method for model generation. This technique consists of assembling SPICE primitives to describe a complex electrical function. Figure 7 depicts the general model we have adopted.

The model works as follows: if the voltage applied to the tube is lower than its cold striking value, no current will circulate

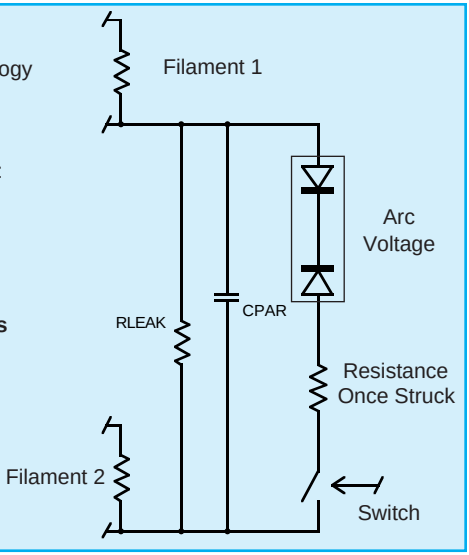

Figure 7 - The subcircuit topology for the fluorescent tube.

The switch is controlled by the following If-Then-Else function:
If V_Tube > V_Strike Then
  If I_Tub > I_Sus Then
  On
Else Off.

An example tube model is available from the Intusoft Web site at www.intusoft.com

except in the leakage elements. If the voltage is further increased and the striking voltage is reached, the voltage-controlled switch closes and the back-to-back zener network is connected across the tube. The voltage then collapses to the arc value and a current flows inside the tube. The tube will stay conductive until the current falls below the sustaining value. At this point, the switch opens and the tube needs to be restruck. The netlist is written for the IsSpice4 simulator and uses standard SPICE 3 elements combined with one of the IsSpice4's SPICE extensions, an If-Then-Else behavioral element.

As previously stated, preheating the filaments decreases the striking voltage. The model accounts for this specific behavior and monitors the RMS current flowing through the filaments prior to the first cold strike. To take advantage of this feature, you should include the UIC (Use Initial Conditions) keyword in the transient SPICE statement (.TRAN *tstep tstop* **UIC**). In AC applications, where the frequency of operation is fast enough, the thermal effects ensure a restrike voltage close to the arc value. This is especially true for high-frequency systems, e.g. electronic ballasts. The BDIFF element (see the netlist posted on the Intusoft web site) models this effect in a simplistic way. Figure 8 shows the I/V characteristics of the IsSpice4 fluorescent tube model, where the negative effects are clearly depicted.

A low frequency AC test using the tube model in a classical 50Hz application is shown in Figure 9. Figure 10 reveals the simulation results.

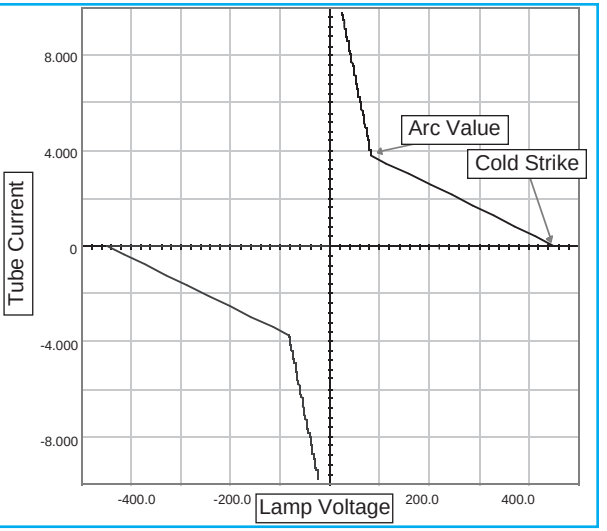

Figure 8 - The DC I/V characteristics for the fluorescent tube model.

To operate the tube model at higher frequencies, you can simply remove the "*" comment symbol in front of the RSTK element in the netlist and place one in front of RNEG, DSTK1 and DSTK2 elements.

A typical application for a self-oscillating ballast is shown in Figure 11. RSTK can be calculated from the RMS lamp operating parameters: RSTK = VARC/INOM. For a 36W tube, RSTK = 103/.43 = 240W.

In this second example, two MOSFETs are driven by a saturable current transformer, using the IsSpice4's nonlinear magnetic core model. The start-up is driven by R17&C12 which forces X21 to enter the conduction mode a few milliseconds after the mains are applied. Square waves are delivered to the non-damped L1-C13 network and a high voltage appears across the tube ends. C13 also ensures preheating of the filaments. Once the tube is struck, the resulting load changes

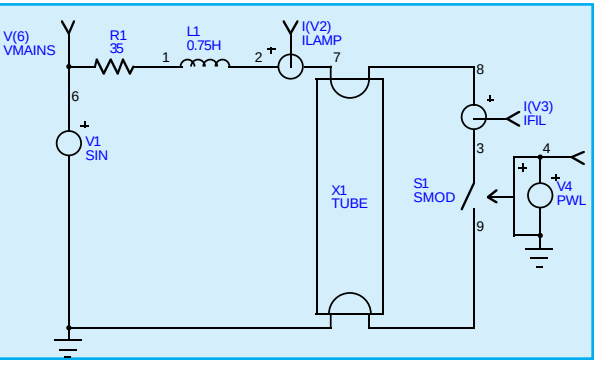

Figure 9 - Tube simulation in a classical 50Hz application. V1 is a sinusoidal waveform. A piecewise linear waveform is used to control the switch.

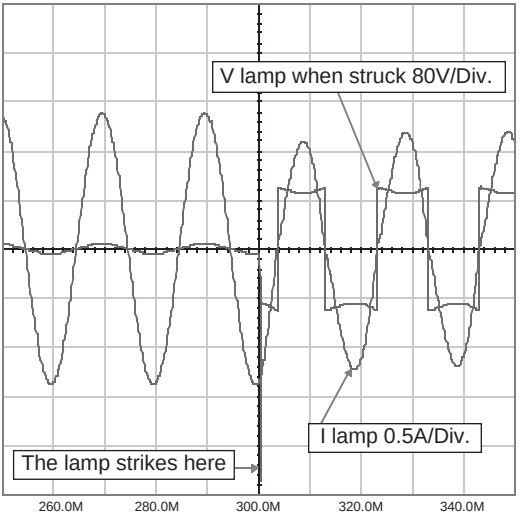

Figure 10 - The simulation results for a low frequency AC test using the tube model in a classical 50Hz application. The lamp is struck when the PWL source causes the switch to close.

the operating frequency of the ballast. Figure 11 shows the IsSpice4 simulation results cross-probed on the schematic.

The model presented here runs fast and converges without difficulties in low and high frequency applications. Thanks to its macro-modeling structure, operating parameters can be easily adapted to various lamp types. Reference 2 gives further insight into the self-oscillating ballast technique.

References

1. The SPICE book, Andrei VLADIMIRESCU, John WILEY & Sons, 0-471-60926-9
2. Energy Efficient Semiconductors for Lighting, MOTOROLA, Application note BR480/D

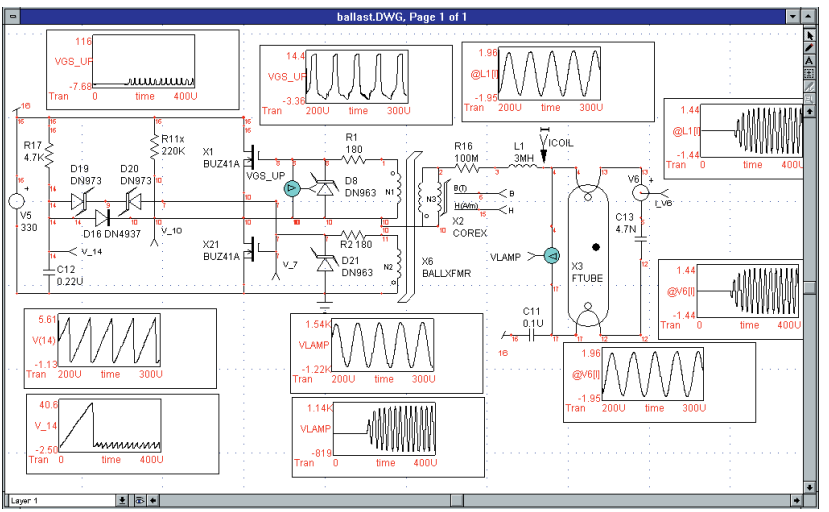

Figure 11 - The transient response of the self-oscillating ballast circuit. Two views of the results can be seen; 0-400us and 200us-300us.

RF/MICROWAVE ANALYSIS

by Karl Heinz Muller

SPICE is a powerful tool that offers the RF engineer significant benefits. **SPICE really has no frequency limitations**; the only issue is how the models perform at the frequencies of interest. The SPICE linear analyses are comparable to those found in many linear simulators, while the nonlinear strength of SPICE can reveal important circuit behaviors that linear simulators do not. For instance, IsSpice4 has models for stripline/microstrip, lossy transmission lines with skin effect and dielectric loss, plus models for PIN diodes, MMICs, GaAs Mesfets, RF BJTs, Beads and more; all of which can be simulated in both the time and frequency domains.

As a simple example, we'll look at a negative resistance amplifier. This circuit is used at higher microwave frequencies

```
.SUBCKT CIRCULATOR  1  2  3
E1 5 0 1 4 1MEG
E2 7 0 2 6 1MEG
E3 9 0 3 8 1MEG
R1 4 9 50
R2 1 9 50
R3 4 5 50
R4 5 6 50
R5 2 5 50
R6 6 7 50
R7 7 8 50
R8 3 7 50
R9 8 9 50
.ENDS CIRCULATOR
***
.SUBCKT TUNNELDIODE  1  2
*1N3858 Vp=55-95mV Ip=9.5-10.5mA Vv=350mV
*Iv=1.2mA Vf=510-580mV RS=2.5Ohm Cj=8P
R1 1 3 2.5
I0 3 2 1.2M
D1 3 2 DIODE
J1 4 2 3 NKANALJFET
J2 4 3 2 PKANALJFET
.MODEL NKANALJFET NJF (VTO=-.115V BETA=1.9 CGS=4P)
.MODEL PKANALJFET PJF (VTO=-.115V BETA=1.9 CGS=4P)
.MODEL DIODE D (RS=7 N=.6)
.ENDS TUNNELDIODE
```

Figure 12 - The subcircuit netlists and topologies for the circulator and the tunnel diode. The parameters for the 1N3858 diode are shown.

where appropriate field effect and junction transistors are not available. Here, the circulator coupled negative resistance amplifier is a possible alternative. The ferrite circulator (Figure 12) is a non-reciprocal device having low insertion loss in the clockwise direction while counterclockwise ports are isolated. Negative resistance may be generated by two-terminal semiconductors like gunn, impatt, or tunnel diodes. In the following example, a tunnel diode is used for small signal

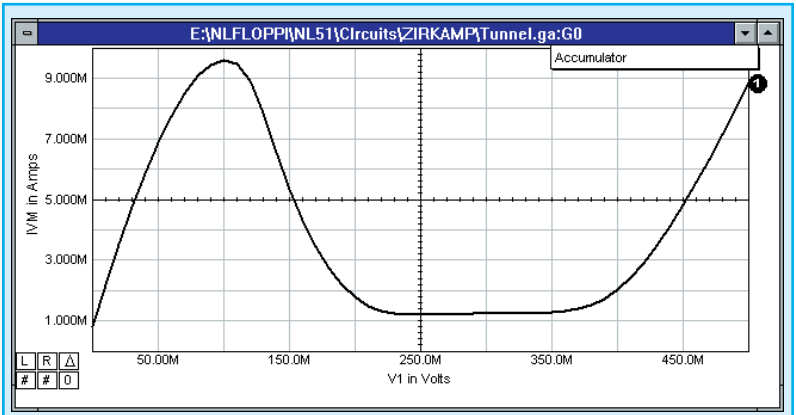

Figure 13 - The DC characteristics for the 1N3858 tunnel diode. Note the negative resistance region produced by the complementary JFETs.

amplification. Tunnel diodes are occasionally found in military equipment, where insensitivity to nuclear radiation and wide temperature changes are required.

A negative resistance is characterized by an increase in voltage with a proportional decrease in current. Modeling of the tunnel characteristic is not easy. A cubic polynomial approximation

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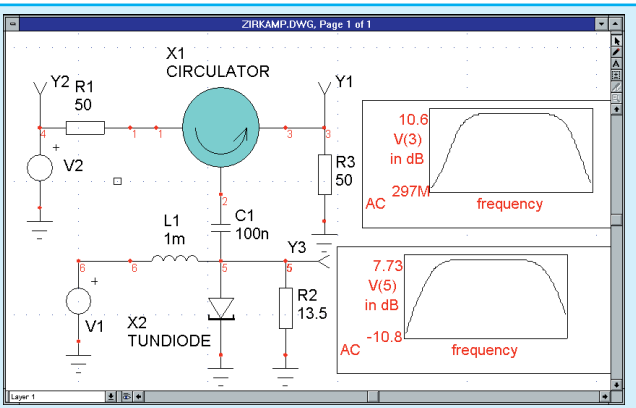


Figure 14 - A negative resistance amplifier made up of a circulator and a tunnel diode. Cross-probed waveforms show the frequency (Bode) response.

SIMULATION TOOLS FOR PROTEL

The most powerful and easiest-to-use simulation tool for Protel® Advanced Schematic™ users is now available. The wait for seamless integration AND state-of-the-art simulation power is over!

ICAP for Protel adds a full suite of simulation tools to Advanced Schematic including the proven IsSpice4 analog and mixed-signal simulator, extensive model libraries, a powerful waveform analysis tool, and a host of features that make simulation easy to perform.

ICAP uses the EDA Client/Server architecture, Protel's powerful integration technology and OLE (Object Linking and Embedding) to transparently integrate the powerful features of the ICAP/4 Virtual Circuit Design Laboratory into the Protel schematic environment.

ICAP Integrates Using EDA/Client

The EDA/Client server technology was created to allow packages from different vendors to be integrated (with equal levels of integration regardless of the developer) with Advanced Schematic.

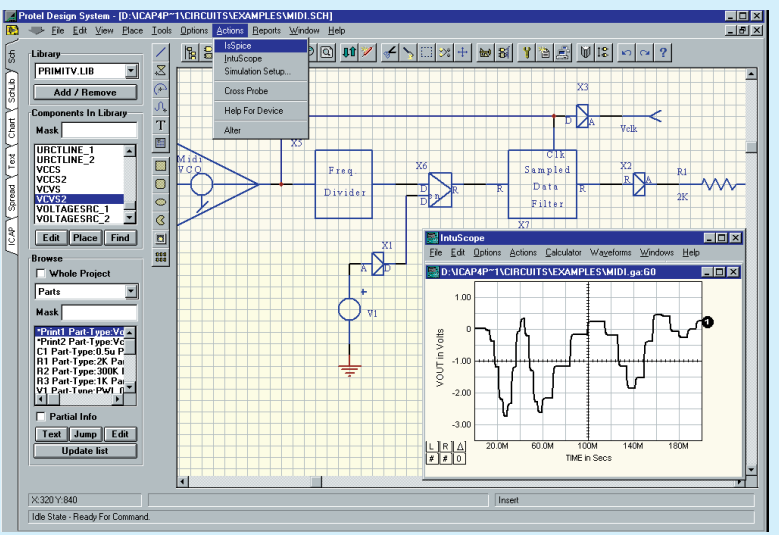


Figure 15, The ICAP system is seamlessly integrated into Protel's Schematic[3] using the innovative **EDA/Client** environment. Here we see the new menu functions added to Advanced Schematic which allow you to simulate directly from the schematic.

ICAP for Protel is vastly superior to Advanced Sim3

Feature Description	ICAP	Advanced Sim3
Seamless Integration using EDA/Client	✔	✔
Built-in mixed-signal simulation	✔	✔
Full SPICE 2 and 3 compatibility	✔	Limited Spice3
More Analyses: Everything in Advanced Sim3 plus Failure, Curve Family, Sensitivity (AC/DC), PZ and Distortion analyses	✔	Limited
Over twice as many models;13,000;	✔	6,400
SPICE Model Types	Over 400	<50
Cross-probing (Voltage, Current, OP & Power)	✔	Limited
Waveform Processing and Analysis Tool	✔	Very Limited
Interactive SPICE with OLE/VB Scripting Language	✔	No
Analysis and Convergence Wizards	✔	No
Power, RF, and Mechatronic Model Libraries	✔	No Power/RF
Parameter Sweeping and Curve Family Generation	✔	Limited
Tutorial Movies To Get You Going	✔	No
Behavioral Modeling	✔	Limited
On-line Help	✔	???
Support/Free Modeling Service	✔	???
Installed based of seats	18,000	500

Using EDA/Client means ICAP for Protel works closely with Protel's Advanced Schematic; integration so tight the two programs appear to be from one vendor. With a single-click on the schematic you can cross-probe voltage, current, operating or power dissipation waveforms. A new Actions menu has been added to Advanced Schematic that allows you to simulate directly from the schematic.

AS shown in the table above, ICAP for Protel includes a large number of features that Advanced Sim does not. ICAP for Protel's superiority comes from the feature set added to Advanced Schematic and advanced simulator features.

In addition to its native analog and gate-level digital simulation capabilities, ICAP for Protel includes support for BSIM3v3 and SOI MOSFET models. The tool also supports SPICE libraries with over 13,000 analog and digital (CMOS, TTL, ECL) parts, as well as, an AHDL modeling capability, Special RF, Power and Mechatronic SPICE model libraries are also offered.

The interactive operation of ICAP for Protel frees the user from traditional batch-style SPICE simulators. High-performance algorithms provide very fast simulation and improved convergence for difficult circuits. IsSpice4's advanced features

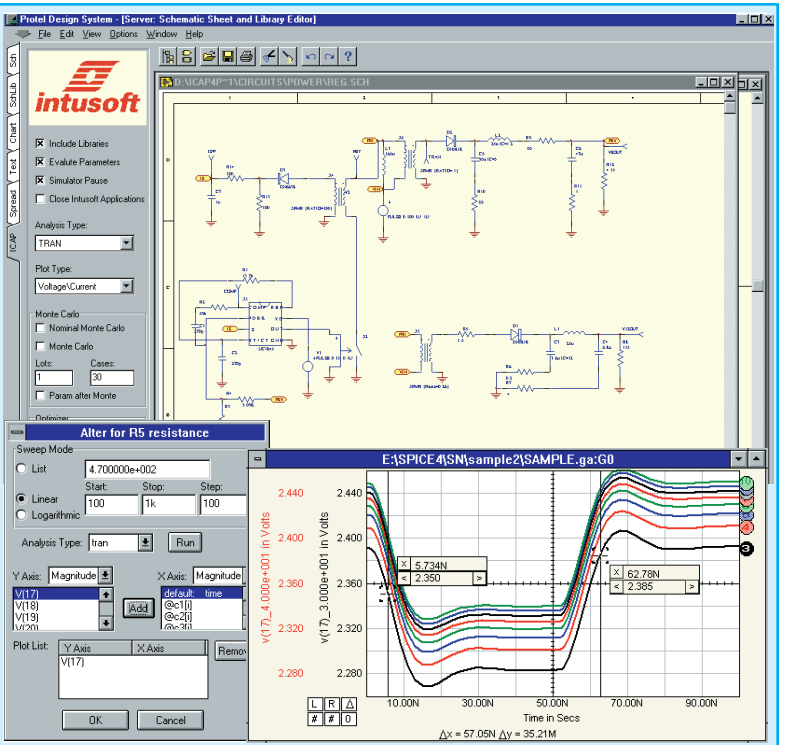


Figure 16, Powerful Parameter Sweeping, ICAP for Protel adds specialized dialogs that give you the power to sweep circuit variables and create curve families.

include: behavioral modeling, sweeping of any circuit variable; native mixed-signal simulation; interactive waveform cross-probing, automatic curve-family generation, and real-time display of voltages, currents and power dissipation. ICAP for Protel can analyze switch-mode power supplies, mixed-signal ASICS, RF communication systems, PCB interconnects, control systems, and mixed electrical/mechanical/hydraulic systems.

With analog simulation, support can be a critical issue. In time of need you need a company that can model parts for you and understands your problems. Intusoft has been handling SPICE related problems for over 12 years. Make sure your vendor can handle the technical aspects before buying!

ICAP for Protel is available immediately.
For more information contact intusoft or your local intusoft dealer.

SIDACTOR MODELING

by A.F. Petrie

A SIDACTOR is a bilateral switch, similar to a triac, without a gate connection. It can be triggered into conduction regardless of polarity, but only by an overvoltage pulse. Sidactors are often used as overvoltage protection devices with clamping voltages from 20 to over 500 volts.

Upon application of a voltage exceeding the breakdown voltage, the sidactor switches on through a negative or positive resistance region to a low on-state voltage. Conduction will continue until the current is interrupted or drops below the minimum holding current. The sidactor can offer longer life and faster response (nanoseconds) than other types of protection and is able to respond without voltage overshoot. The sidactor is as fast as a zener diode, while offering a much lower impedance (leakage current <5ua) during conduction.

The latest version of the powerful SpiceMod (v2.4.3) modeling program allows you to create SPICE models for sidactors from data sheet parameters. The program takes the data sheet parameters and converts them to the appropriate SPICE model parameters. The subcircuit topology and an example netlist are shown in Figure 17. The netlist uses a SPICE 2G.6 format and is compatible with all commercial SPICE-based simulators.

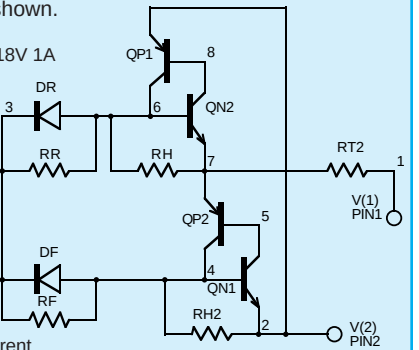
The sidactor is modeled by using two NPN/PNP transistor pairs. The base of each transistor is connected to the collector of the other. This produces positive feedback, resulting in the required switching action. Resistors and zener diodes are used to simulate the breakdown voltages and leakage currents.

Because these devices have two stable states, you may need to tell SPICE which state to use. This is accomplished by including the “OFF” parameter on the subcircuit transistors. This will set up an initial starting condition in the normal starting state.

The chief causes of SPICE convergence problems are due to abrupt changes in a circuit’s impedance. To aid IsSpice4 in converging during the abrupt sidactor switching, the following OPTIONS statement is recommended “.OPTIONS ITL1=400 ITL4=500 RELTOL=.005.

It should be noted that these are the options chosen by the Convergence Wizard feature, included in ICAP/4 version 8, when a mild convergence problem is encountered.

Figure 17, The IsSpice4 netlist for a sidactor. The parameters for a Teccor K1100E70 118Volt 1Amp device are shown.




```
*K1100E70;K1100E70;Sidacs;TECCOR; 118V 1A
.SUBCKT K1100E70  1  2
*     TERMINALS: MT2 MT1
QN1  5 4 2  NOUT; OFF
QN2  8 6 7  NOUT; OFF
QP1  6 8 2  POUT; OFF
QP2  4 5 7  POUT; OFF
DF  4 3  DZ; OFF, Forward breakdown
DR  6 3  DZ; OFF, Reverse breakdown
RF  4 3  1.18E+10 ; controls IBO
RR  6 3  1.18E+10
RT2 1 7  0.755 ; controls "on" resistance
RH  7 6  11.5 ; controls holding current
RH2 4 2  11.5 ; controls reverse holding current
.MODEL DZ   D (IS=321F RS=100 N=1.5 IBV=10N BV=118) ; controls VDRM
.MODEL POUT PNP (IS=321F BF=10 CJE=134N TF=25.5U)
.MODEL NOUT NPN (IS=321F BF=20 CJE=134N CJC=26.8N TF=1.7U)
.ENDS
```

The following NPN/PNP parameters control the performance of the sidactor at high speeds (high dv/dt):

CJE = Controls the high speed triggering, CJC = (with RS + RGP) controls the maximum forward voltage application rate (dv/dt) before triggering occurs, and TF = Ideal Forward Transit Time (not fall time). This determines the turn-on and turn-off time

Figure 18 shows a sample application where a sidactor is added to protect a transistor during inductive load switching. Several sidactor models are included on the newsletter floppy disk and are posted on Teccor's web site at www.teccor.com.

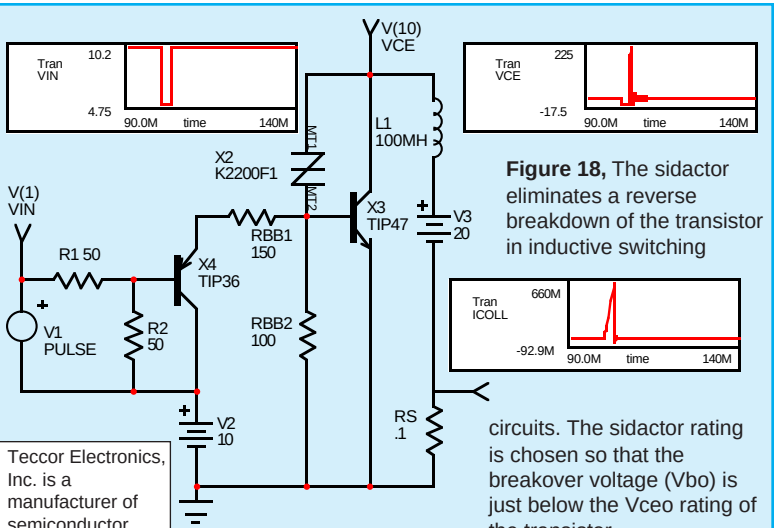


Figure 18, The sidactor eliminates a reverse breakdown of the transistor in inductive switching circuits. The sidactor rating is chosen so that the breakover voltage (Vbo) is just below the Vceo rating of the transistor.

Teccor Electronics, Inc. is a manufacturer of semiconductor devices.

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computing directly from your ICAP/4 Simulation Control Panel. Now you can run failure or Monte Carlo analyses **50 times faster** than your typical desktop 200MHz Pentium.

The power is transparent. By default, you'll use your local computer to simulate. But push the "Remote SPICE" button, and your instantly connected to a state-of-the-art "super computer" that turns simulation days into minutes. For example, a failure analysis of 300 - 1 minute simulations which takes 5 hours on a 200MHz pentium will run in under 6 minutes! The SpiceFarm server spins off jobs to an array of "Worker" computers. Each worker is a Pentium II 266 or better with 128 Meg of RAM. As tasks are completed, the results are returned to the user.

Our 1st quarter '98 maintenance release for the Design Validator and Test Designer products will include this feature, along with **25 Tera-ops of complimentary computing** power using the Web accessible SpiceFarm located at Intusoft's home office. Additional Internet service can be purchased in 100 Tera-op increments. A SpiceFarm that connects to your LAN will be available for purchase in March of 1998. Please call or email Intusoft for further details.

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IsSpice4 provides a quantum leap in performance over other analog and mixed mode simulators. It is the first commercially available version of SPICE based on Berkeley SPICE 3F and Georgia Institute of Technology's XSPICE.

IsSpice4 allows you to explore circuit performance by interactively running different analyses and sweeping any circuit variable. With the ability to simulate electrical, sampled-data, mechanical, physical, thermal, and other systems, **IsSpice4 is the ONLY true native mixed mode SPICE 3 based simulator.** The advanced features of IsSpice4 allow all types of applications to be simulated: switch mode power supplies, mixed signal ASICs, RF communication systems, interconnects, control systems, and mixed mechanical/physical systems.

Intusoft has spent thousands of man-hours improving SPICE. And although IsSpice4 is based on SPICE 3, Intusoft has greatly enhanced the program over and above the public domain version; adding an interactive interface, providing superior analysis and model support, and improving the convergence algorithms - all for a price no one can match. IsSpice4 is simply the best and most affordable SPICE program on the market today. Just take a look at some of its features:

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- **NEW VISUAL BASIC SCRIPTING** - Drive IsSpice4 using VB scripts from popular programs like Excel.
- **NEW OLE INTERFACE** - Develop your own OLE/ActiveX interfaces

Built-in Models

- Elements: Resistors, Capacitors, Inductors, Coupled Inductors, Transmission Lines, Diodes, BJTs, JFETs, MOSFETs (Level 1-8), GaAs Mesfets, Switches, and Boolean logic expressions.
- Digital and AHDL Models: Digital primitives, State Machine, Frequency Divider, RAM, Sampled-Data Filters, Nonlinear VCOs, Laplace Equations
- Behavioral Modeling: In-line Equations, Table models, If-Then-Else

Advanced Models

- HDL Models and C Subroutines; Create models based on a powerful nonproprietary HDL using C
- Support for nonelectrical applications and top-down system design
- Three types of digital/mixed mode modeling
- Lossy (distributed) transmission lines with frequency dependent losses
- MOS: BSIM1, BSIM2, BSIM3 version 2 and 3.1 and SOI MOSFET models
- MESFET: Statz, Curtis-Enttenburg, Parker-Skellern, and HEMT models

Analysis Support

- AC, DC, transient, noise, Fourier, distortion, DC/AC sensitivity, Pole-Zero analyses, and Temperature variations on individual elements
- Monte Carlo Analysis, Circuit Optimization/Performance Analysis
- ***NEW DESIGN VALIDATOR***™ for automatic design verification
- ***NEW TEST DESIGNER***™ Fault Analysis and Software Test Set Design

Additional Interactive, AHDL & Mixed Mode Features

- Real-time Display of voltages, currents and power dissipation
- Simulation Scripts: a robust scripting language that allows simulation breakpoints and loops of different analyses to be run as a test procedure.
- Interactively run analyses without having to edit the netlist or restart the simulator, add, delete, or rescale waveforms on the real-time display
- Digital Simulation: IsSpice4 includes a 12 state digital logic simulator and models with timing information
- Sweep parameters one at a time or in groups with great ease
- Start, stop, pause, change, or resume any analysis on demand
- Use C code subroutines & AHDL models based on XSPICE

Convergence and Speed Improvements

- Automatic Gmin stepping/Source stepping algorithms
- New Pseudo-Transient algorithm
- Improved Predictor-Corrector, Latency, and Bypass algorithms
- Improved program defaults
- Special Circuit Debugging Options
- Full Gear Integration option

Compatibility

- True OLE Integration with popular schematic entry programs
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DID YOU KNOW INTUSOFT WAS THE FIRST?

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- **SPICE 2 Models for:** IGBTs, fuses, lasers, vacuum tubes, generic template models, dual gate Mosfets, SC filters, neural networks, digital gates, RF beads, IBIS buffers, saturable cores, and PWMs (using the state space approach)

- **Products/Features:** Monte Carlo analysis for PC-based SPICE, integrated schematic entry dedicated to SPICE, SPICE 2 compatible model generation software, 32-bit version of SPICE for DOS, support for all Macintosh platforms, parameter passing

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Affordability is the hallmark of Intusoft's products. With our new ICAP/4Rx, ICAP/4Windows, and ICAP/4Macintosh software, all affordably priced, there's an IsSpice that's just right for you.

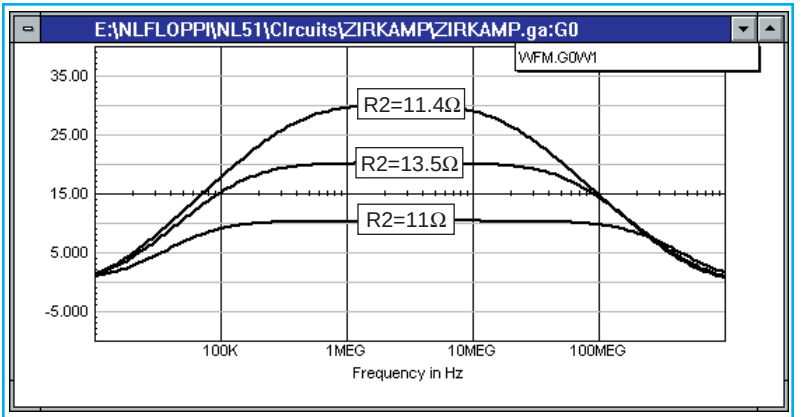

Figure 19 - A Bode plot showing the gain of the negative resistance amplifier in Figure 14 vs. frequency for several values of R2.

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suffers from accuracy problems. This could be improved by using polynomials of higher orders, but simulations have shown that remote curve branches will then lead to ambiguities. The best results are found with a connection of two complementary JFETs, as shown in Figure 12. The tunnel diode's DC response is shown in Figure 13.

Stability is a critical point in negative resistance amplifiers. If the negative resistance approaches -50 Ohm, the amplifier starts to oscillate. To achieve a minimally stable condition, an ohmic resistor is connected in parallel. The amplifier and AC response are shown in Figure 14, while the frequency variation with resistor R2 is shown in Figure 19.

New Models From Vendors

The *Intusoft Newsletter* floppy contains a variety of new models from several manufacturers including: Connector models from AMP, and Op-amps, full bridge Power Mosfet drivers, MOVs, and Power Mosfets from Harris. Some of the Mosfet models include radiation hardening and temperature effects.

Several new PWM models are also included for the Unitrode UC1846, UC1871, and UC1872, the Motorola MC33363 and 78S40, the SGS-Thomson L4990 and the Allegro STR6600. Lastly, generic voltage and current mode PWM controllers using both an AHDL/mixed-signal modeling approach and analog behavioral approach are included. Technical articles on these models are available on the Intusoft web site.

The models are available by subscribing to the *Intusoft Newsletter*. ICAP/4 and ICAP users will also recieve these models via their software maintenance updates.