

# Intusoft Newsletter

Personal Computer Circuit & System Design Tools



Copyright © Intusoft, All Rights Reserved

Issue #73 Feb. 2004  
Tel. (310) 329-3295  
Fax (310) 329-9864

## ICAP/4 Continues to Grow in 2004

In the second half of 2003, Intusoft created a formal method to gather data from the analog EDA market, and from customer feedback, to determine what software enhancements were most desired for ICAP/4. The primary outcome led us to increase ease of use and add more intuitive features to the software.

In the latter half of 2003 we implemented several features to improve the functionality within ICAP/4. For example, the schematic interface was greatly improved through things like rubberbanding, which enables movement of a component, or group of components, without breaking associated wiring connections. The ability to rotate or flip multiple parts as a “group select” was another prominent feature. Another enhancement to the software was the ability to move the crossprobe cursor over a schematic plot, and have this cursor automatically change to the normal cursor while it is over the plot. This enables easy moving, deleting, and resizing of plots without changing cursors between operations.

So now we’re ready to continue our journey of enrichment into ICAP/4 by propelling to this Summer’s release.

**Continued on Page 8...**

### In This Issue

- 1 ICAP/4 Continues to Grow in 2004**
- 1 Behavioral Models - Limitations**
- 2 Voltage Controlled Oscillator**
- 3 Voltage Variable Capacitor**
- 4 Modeling Comparators**
- 6 Modeling Amplifiers with Limits**
- 7 Building Hierarchical Models with Subdrawings**
- 8 New Features For Summer 2004 Release**
- 14 Library Manager Extends to ICAP/4 “Deluxe” Software**
- 15 Intusoft and SiSoft Join Forces with Partnership**

## SPICE Numerical Methods, Part 2 Behavioral Models – Limitations

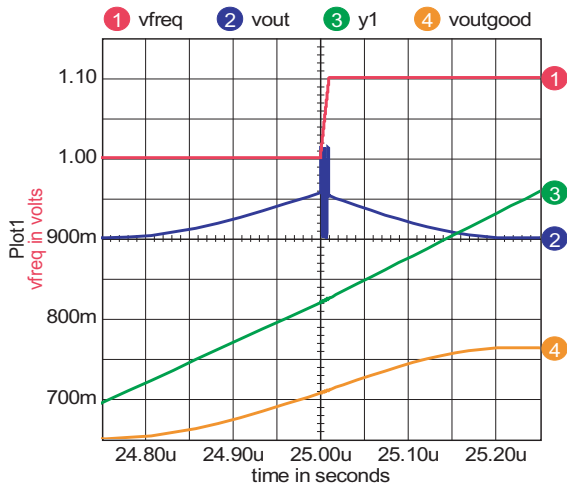
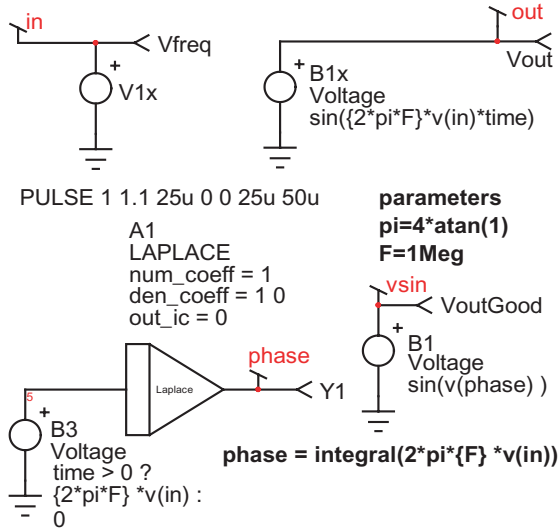
In our previous newsletter we discussed how the IsSpice4 simulator works and made a detailed study of the options that control accuracy and convergence. In this newsletter we will continue by illustrating how to combine the IsSpice4 primitive elements to make commonly needed behavioral models. First we’ll explore, by example, some less than obvious limitations in using B-element expressions.

# Voltage Controlled Oscillator

It's convenient to model an oscillator using a behavioral expression:

$$V = \sin(2 \cdot \pi \cdot v(F) \cdot \text{time})$$

But, if  $v(F)$  is a variable, the interpretation is incorrect as shown below.



**Figure 1:** A voltage controlled oscillator gives unexpected results if frequency is used as a variable instead of phase; phase continuity is required.

As the controlling voltage sweeps from 1 volt (1MegHz) to 1.1 volts (1.1MegHz), the resulting waveform at  $vout$  has high frequency oscillation. But that follows the equation exactly! What we really wanted was to define the output as the sine of phase. By doing that you get the correct interpretation shown in the above graph as  $voutgood$ .

# Voltage Variable Capacitor

In figure 2, we want to make a capacitor change value at a particular voltage, which will model the behavior of a MOS transistor as its gate to drain voltage crosses threshold. The proper interpretation should use charge, not capacitance. When the capacitance value is changed, a voltage discontinuity occurs. If charge is controlled, the expected result is achieved; that is,  $V = Q / C$ . A similar argument can be made for making an inductor vary as a function of current. The integral of voltage, flux, needs to be used or  $I = \int V dt / L$ .

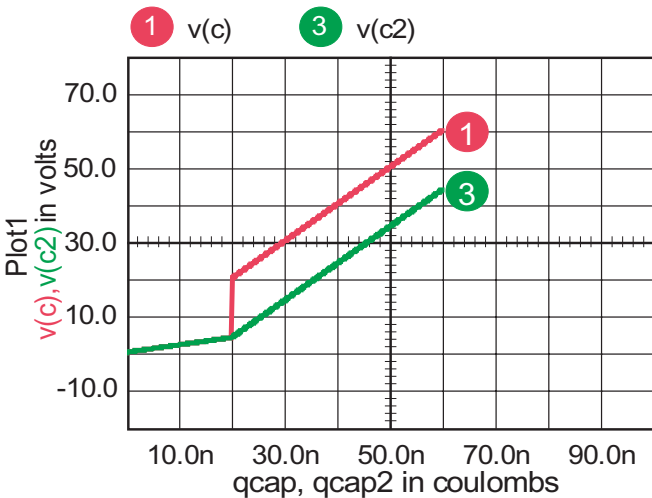
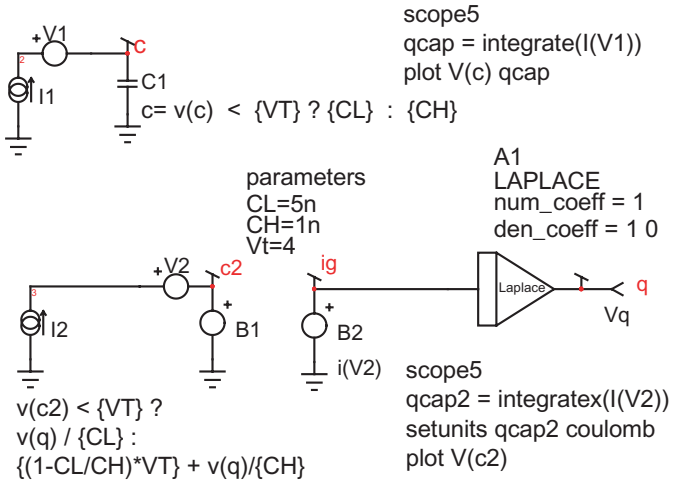


Figure 2: Variable capacitors need charge continuity.

# Modeling Comparators

Comparators are widely used in behavioral models. SPICE2 is severely limited; basically, the diode and gain elements are all that are available. But with SPICE3 there are many more choices. Even the diode method is improved by using small emission coefficient, N, and setting the diode temperature to 27; SPICE2 doesn't allow separate instance temperatures. If you reduce N by a factor of 1000, then the diode looks like a very sharp switch, switching on around 1mv. The disadvantage is that the temperature coefficient of current, when the diode is reverse biased, is too large, and virtually any deviation in circuit temperature makes the model fail. Limiters are modeled as high gain amplifiers that switch from VLO to VHI when the input exceeds VLIMIT. The number of DC iterations to converge, and the existence of derivatives before and after limiting, can judge the quality of the model. Here are three methods to model a comparator.

## Diode Limiter

Figure 3 shows a diode-based model. With N=1m, the accuracy is very good; however, accuracy will suffer if SPICE2 compatibility is required.

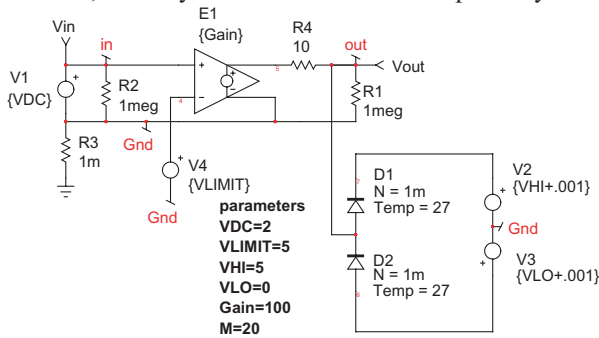


Figure 3: SPICE3 based Diode Limiter.

## If-Then-Else Limiter

The behavioral limiter is the simplest form, shown in Figure 4. It's perfectly accurate; however, the derivatives at limit are zero, which will result in convergence problems. These problems will mount with circuit complexity although judicious NODESETS can help.

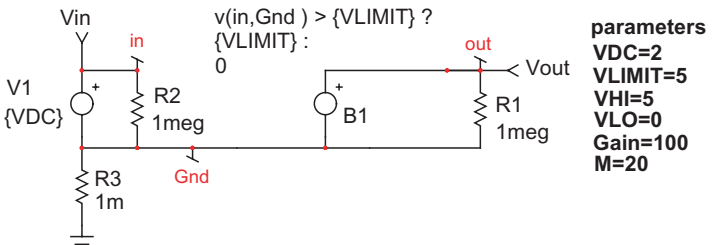
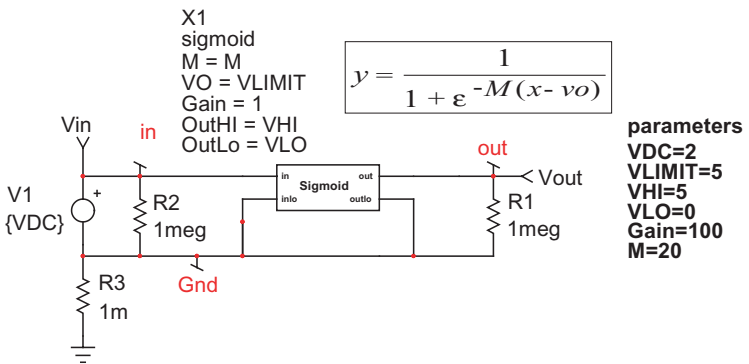


Figure 4: If-Then-Else Limiter has no derivatives to aid convergence.

## Sigmoid Limiter

Sigmoid functions found their way into SPICE models as a result of their use in Neural Networks. The sigmoid equation shown in Figure 5 has the property of being continuously differentiable; although there are practical numerical limitations. For this example, the transition is softer than the diode limiter and derivatives go to zero for a smaller range of the input function.



**Figure 5:** Sigmoid limiter has a smooth transition and a reasonably wide range of derivatives.

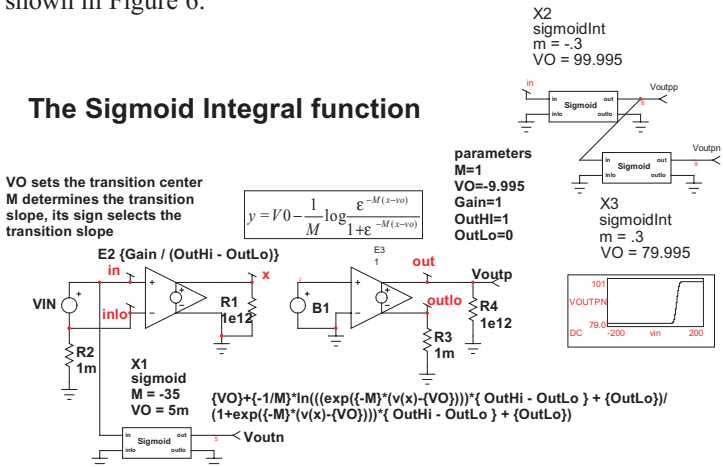
Table 1 compares the 3 models. While the Diode DC convergence isn't as good, the presence of derivatives over a wide range, coupled with its reasonable transition width and accuracy, make it the best general purpose model.

Technique \ Parameter	Diode	If-Then-Else	Sigmoid
DC Iterations	6	3	3
Limit error	1.8m	0	0
Transition width	55m	0	450m
Range of VI for non-zero derivatives	All (20)	0	12.7

# Modeling Amplifiers with Limits

A closely related problem to comparators is the amplifier with limits. The DC behavior of this model sets the stage for convergence in behavioral systems requiring feedback amplifiers. As the signal progresses through a cascade of amplifiers, the simulator is forced to find a tiny window of linear gain. The presence of derivatives over a wide overload range is critical to convergence. Again, the same 3 techniques are used. The only radical change is for the Sigmoid. The function must be integrated before it can be used in an amplifier. The user must do the integration, not the simulator. The new function is shown in Figure 6.

## The Sigmoid Integral function



**Figure 6:** Using the Sigmoid Integral to make an amplifier with limits.

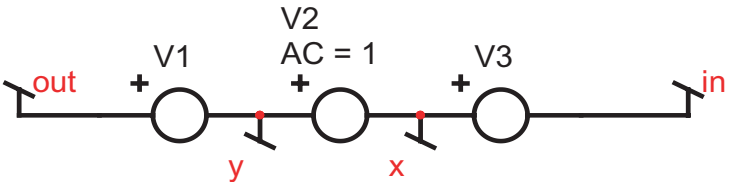
The amplifier with limits was constructed using 2 sigmoid integral functions; one for the positive limit and the other for the negative limit. The 2 subcircuits at the top right of Figure 6 illustrate how a linear output window was constructed with 80 and 100 volt limits. Table 2 compares convergence criteria for the 3 model techniques using a cascade of 2 amplifiers. The first had limits set at (-10,10) volts and the second used (80, 100) volt limits. Remarkably, the model using diodes is far more robust! This can be explained by the broader range of valid derivatives that steer the solution away from the extremes.

Technique	Diode	If-Then-Else	Sigmoid integral
DC Iterations	4	130	7
Max Gain to converge	1e14	1k	1k

# Building Hierarchical Models with Subdrawings

SPICE uses subcircuits to build hierarchical netlists. Intusoft's SpiceNet schematic drawing tool uses a concept of subdrawings to make a hierarchical schematic drawing tree. These subdrawings are each separate schematics, that on the fly are merged with the main drawing as SPICE subcircuits before running a simulation. The advantage of working with subdrawings is that you can probe signals directly down into the hierarchy for debugging. The final model can be converted into a subcircuit using the file\export\Subckt selection.

All SPICE simulators flatten the hierarchical subcircuits before running a simulation. That means that a main circuit node called "out" must also be called "out" as it connects into the subcircuits through the hierarchy. Therefore you cannot use this node in behavioral expressions inside of a subcircuit. Any node in a subcircuit or subdrawing used in a behavioral expression must be buffered. You can connect a voltage source in series or use other SPICE parts as buffers. Models frequently need to be grounded externally; for example, a power supply switching control may need to be grounded on the high side while its output is grounded separately. You can use E elements to convert an input signal-ground pair to a SPICE grounded model, and B elements to connect the output to its own ground. This technique solves the buffering problem as shown previously in Figure 6. Figure 7 shows how voltage sources can buffer internal nodes and how the SPICE3 hierarchical rules can be used to run scripts using subdrawing or subcircuit node names.



**For single injection GFT voltage loop gain  
where the signal propagates from left to right  
Then  $-v(y:xgft) / v(x:xgft)$  is the transfer function  
where the subcircuit must be named  $xgft$ .**

Figure 7: A single injection GFT model and its script

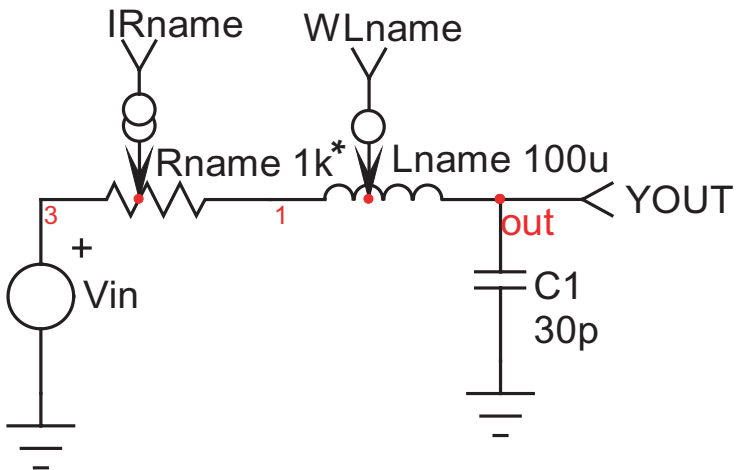
## New Features For Summer 2004 Release

We now delve into the summer release of 2004 by informing you of some of the features developed for this ICAP/4 version. And since ease of use and operability enhancement were at the top of the priority list from our customers, those were the primary areas targeted for this summer.

Let's start with a number of changes added to SpiceNet that make it easier to work on your schematic. In short, voltage, current and power test points now assume the name of a component's reference designation, or a circuit node's name if assigned by the user. This requested feature makes it much clearer to identify test points, and corresponding waveforms, for their specific areas in a design.

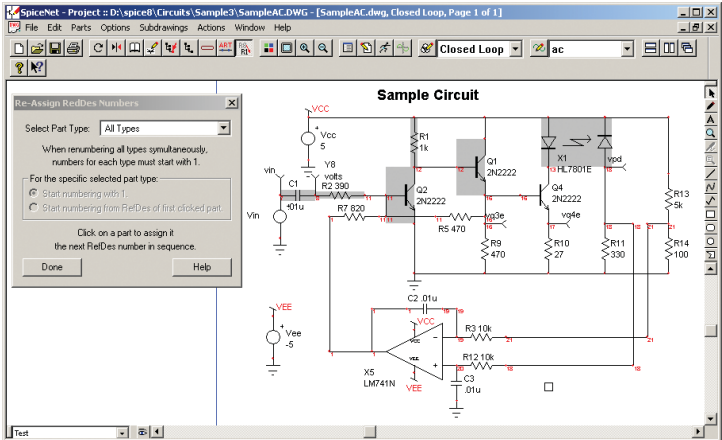
For example, when adding a voltage test point to a named node, the test point's RefDes is set to the name of the node, e.g., named "YOUT" for a node named OUT. If the node is unnamed, the RefDes is set to "Y<n>", where <n> is the node number. When adding a current or power test point to a part, the test point's RefDes is changed to a name that reflects the part it is connected to (e.g., "WR1" for a power test point connected to resistor "R1," "IR1" for a current test point and "IX1\_1" for a subcircuit current test point connected to pin 1 of X1.)

In the example below, a current test point was connected to a resistor, a power test point to an inductor, and a voltage test point to a named node. Notice that the test points are automatically given the same name as the entity they are connected to.

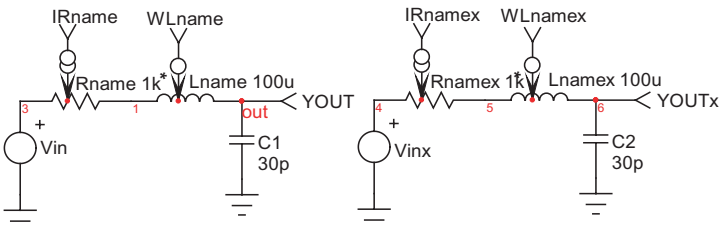




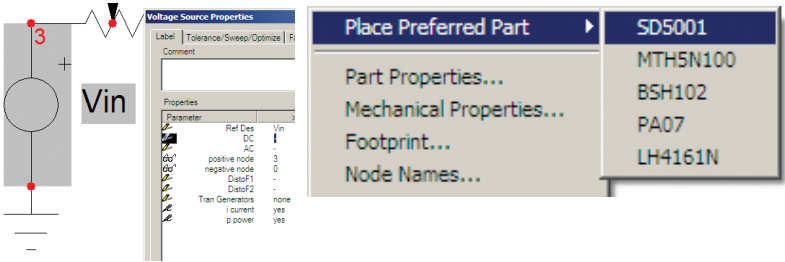
This next feature gives a user the flexibility to easily renumber any or all of a schematic's part reference designations. This provides a more intuitive flow for tracking parts throughout a design and it works as follows. The user selects "Reassign RefDes..." from the Edit menu, or clicks on an optional toolbar button. A non-modal dialog is displayed, which tells the user to click on parts in the desired order, and they will be renumbered sequentially. The default mode is to begin renumbering each type of part starting from 1, e.g., R1, C1, X1, etc. The dialog also provides the capability to start renumbering a specific part type, starting with the first part of that type that is clicked. When a part is renumbered, it is highlighted so the user can remember which parts have been renumbered, and which ones have not. Renumbering stops when the user closes the dialog, either by clicking its "Done" button, reselecting its menu item, or re-clicking its optional toolbar button. Renumbering can be undone and redone, in the same fashion as most other SpiceNet changes.



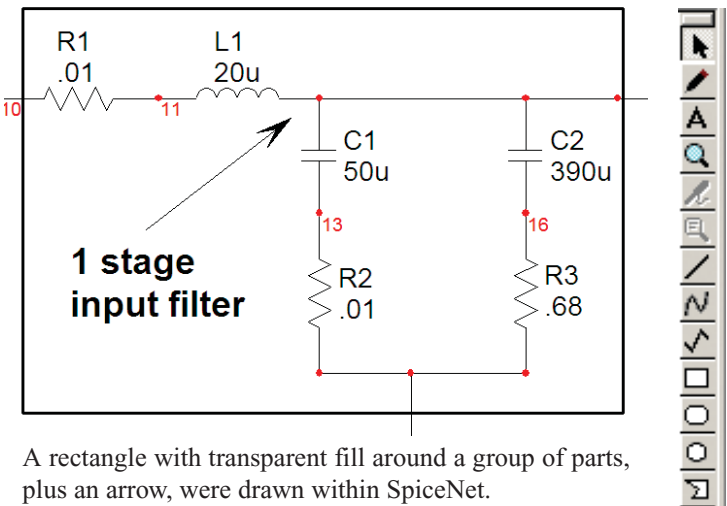
A part's RefDes is retained when copying and pasting, as long as the prior RefDes does not already exist on the target drawing. A RefDes that has been modified to a non-standard form is also retained with one or more 'x' characters appended to its copied one, to distinguish it from the original. In the example below, the RLC circuit was copied and pasted over to the right, including its new test point names.



Also adding to intuitive operations with parts, when a component is double-clicked, any labels belonging to that component are automatically selected. This provides an easy way to verify specific labels unique to their corresponding components. Further, a “Preferred Parts” hierarchical menu has been added to the right-button popup menu. This makes it even easier to quickly place components, and subcircuit parts, since you don’t have to use the Part pulldown menu.



Importantly, a number of capabilities have been added to make SpiceNet more efficient and easier to create high quality schematic drawings, including printouts for documentation purposes. For instance, if you previously wanted to draw simple artwork shapes, such as a dividing line or box around a group of components, you would first have to draw the artwork in the symbol editor and then send it over to the schematic. But now, drawing tools have been added to SpiceNet’s main window, which add simple artwork shapes to the schematic drawing. The ability to group selected artwork and free text labels into single symbols has also been added.



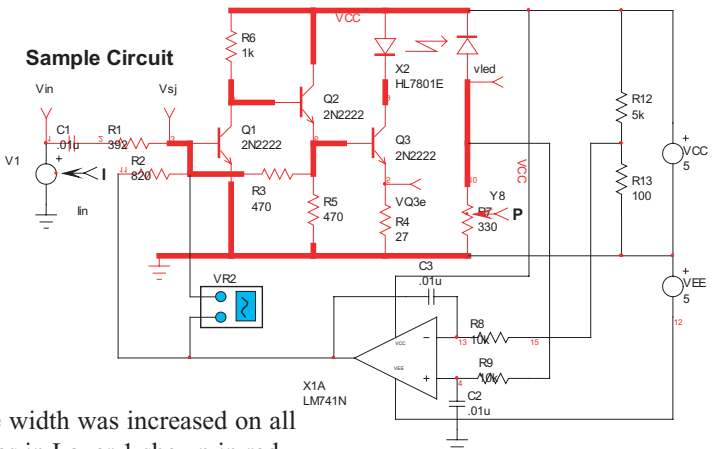
A rectangle with transparent fill around a group of parts, plus an arrow, were drawn within SpiceNet.

New constraint functions have been added to create new artwork shapes much faster. Constraints are achieved by simply holding down the shift key during desired operations. The outcome is as follows:

- Lines are constrained to angles of 0, 45, 90, 135, 180 and 225 degrees. This is applicable for lines, poly-lines, polygons, and base lines for Bezier curves. It applies to both the main window and the Symbol Editor.
- Rectangles, rounded rectangles and ellipses are constrained to squares, rounded squares and circles respectively, in both the main window and the Symbol Editor.
- Elliptical arcs and half ellipses are constrained to quarter and half circles in the Symbol Editor. Drawing arcs and half ellipses are not supported in the main window. In all, much time is saved with the above new capabilities employed by almost any designer.

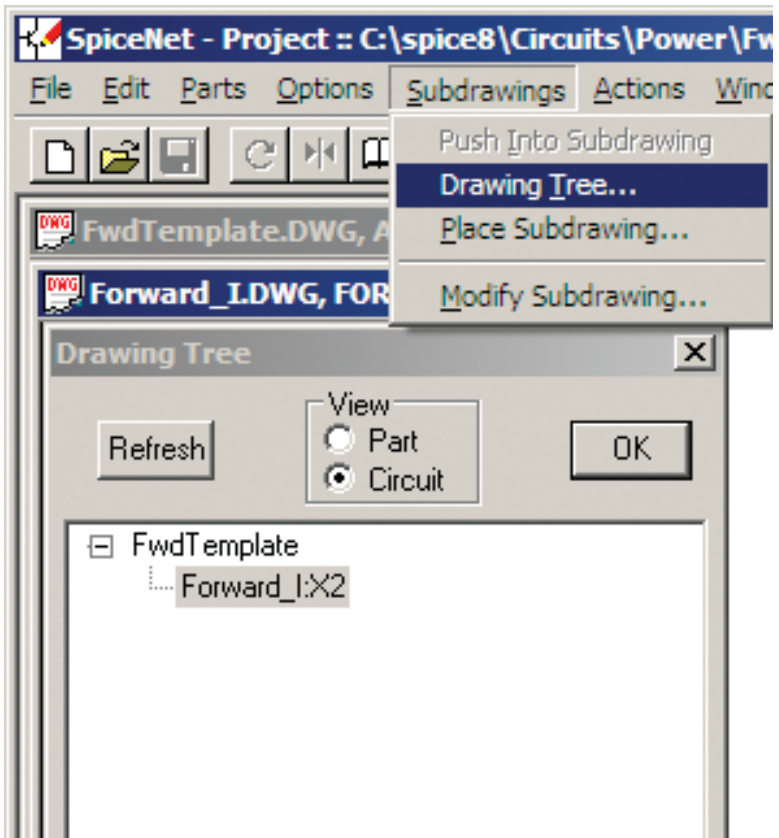
We made mention of the symbol editor; “Save Preferences” and “Restore Default Prefs” have been added to the SpiceNet Symbol Editor Options menu. This makes it possible to save the locations of the Symbol Editor window, tool palette and selected option settings.

Recall that last year we added the ability to adjust schematic wire widths if the schematic was to be printed, or copied to the clipboard and pasted to a target publication. The ability has now been added to modify wire widths displayed in SpiceNet. This enables improved wire visibility and differentiation, if desired. Simply go to the "Options/Drawing" menu and select “Displayed Wire Width...” This dialog can be used to set the displayed width of selected wires, or if none are selected, all wires drawn in the future. Wire widths are not scaled when the drawing is rescaled on the monitor.

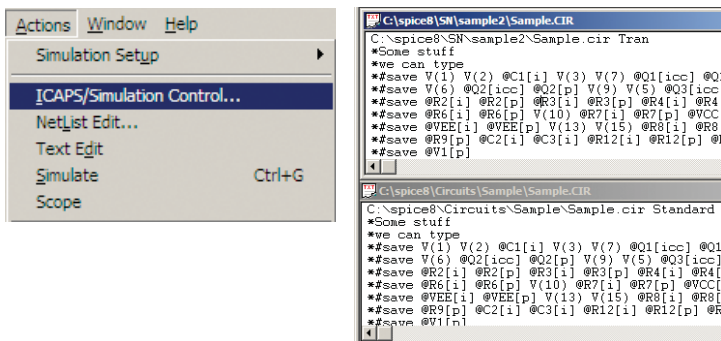


The width was increased on all wires in Layer 1 shown in red.

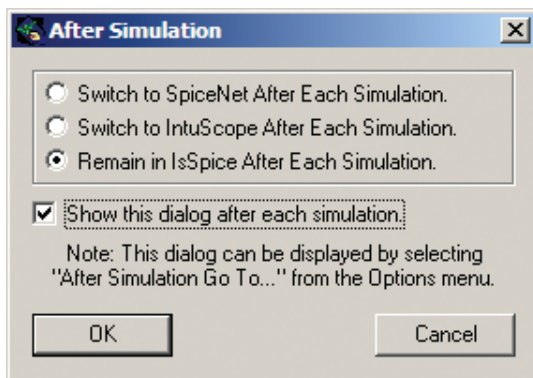
A few changes have been invoked to make it easier when working with subdrawings. First, the “Subdrawings” menu located under the “File” menu has been moved to the main menu to replace the “Instance” menu. This was done because the “Instance” menu was rarely used. Next, if the current drawing is a subdrawing of the active project, and you attempt to run a simulation, you are now asked whether you want to simulate the current project, or change the project to the active window before simulation. Therefore, it is no longer necessary to navigate back to the project window before simulation. If the current drawing is not a subdrawing, the project is changed automatically, as before. Finally, if the current drawing is a subdrawing of the active project and you attempt to display a project tree, you are now asked whether the root of the tree should be the active project, or if the active project should be changed to the current drawing before displaying the tree. If the current drawing is not a sub-drawing, you are asked whether you want to change the project or cancel. All these features enable much clearer navigation through drawings and projects, thus saving much time and potential confusion.

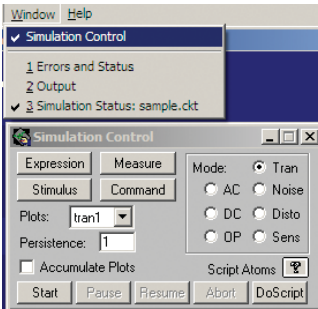


Next, we venture into the simulation environment of ICAP/4. There's no shortage of enhancements added here to enable a more intuitive simulation process for the user. For example, the Actions menu "ICAPS" has been changed to "ICAPS/Simulation Control." This matches the corresponding "simulation control" dialog box that comes to view. Also, in IsEd, the user may elect to have either the full pathname or only the file name appear in window title bars. This makes it easy to determine where the file being worked on is located.



Here's an incredibly valuable feature for this summer's release. Importantly, it enables a user to specify whether the schematic or waveform viewer becomes active immediately following a simulation. If the waveform viewer is chosen, then operations such as "same waveform update" and "crossprobing" save a mouse click per each round of a schematic-to-waveform debug cycle, since you don't have to first select the waveform viewer as before. Here's how it operates. A dialog has been added to IsSpice4, which is displayed after a simulation is run. It has three radio buttons providing the choices: "Switch to SpiceNet After Each Simulation," "Switch to IntuScope After Each Simulation" or "Remain in IsSpice After Each Simulation." There is also a check box for "Show This Dialog After Each Simulation." The Options menu provides an alternate means of displaying the dialog.

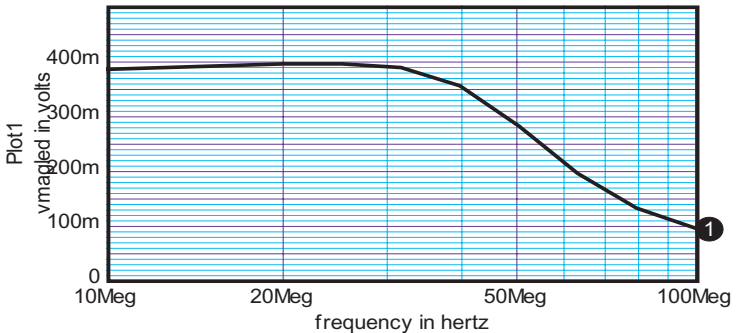




Other operability improvements allow you to Click the Close button on the “Simulation Control” dialog banner to hide it, which now leaves IsSpice4 running. We found that many of our new users would close this window, only to discover the simulation session would completely go away. Also, anytime the dialog is not visible, selecting it from the Windows menu will restore it.

Switching gears to IntuScope, major division lines and labels are shown for logarithmic plots that possess three or fewer cycles at intervals of 1, 2, and 5. The current version has major division lines only at the beginning of each cycle (i.e., at intervals of 1).

① vmagled



## Library Manager Extends to ICAP/4 “Deluxe” Software

In case you don’t know what Library Manager is, it’s a program that compares new models with archived versions, checks for duplicate parts, places new models into test drawings and updates the specified model library. But formerly, Library Manager was only available with Test Designer, ICAP/4 Professional and Magnetics Designer. Good news; its capability will soon be offered in the ICAP/4 Power Deluxe and RF Deluxe packages.

Library Manager adds a TEST button to SpiceMod. Click this button to invoke Library Manager. Then, launch the corresponding test circuit. Library Manager will automatically replace the “Device Under Test” with your new model created by SpiceMod. This allows you to quickly compare simulated measurements and waveforms with the ones from the datasheet.

Library Manager also adds two methods of adding a new SPICE model. Method 1 is to go to a website, copy to clipboard the .subckt or .model netlist, and have library manager import the model from clipboard. Method 2 is to download a file from the web with your .subckt or .model netlist, and have library manager import the model from the file.

**Library manager features:**

- Archive models before you start modifying them so you can revert back to the original version if necessary.
- Compare Library Files so you can see at a glance if a library file has been modified after a software update.
- Compare any two files with character-by-character capability. Easily see before and after edits. New text is show in blue underline and deleted text is show in ~~red-strikeout~~.
- Safely and easily modify the part number, part type, sub type, notes, etc. with library manager's easy interface.
- Modify node names on the .subckt line and the same node name throughout the netlist will change to the new node name. For example: nodes 1, 2, 3, 4, 5, 6 and 8 can be changed to Adj, FB, CS, Gnd, Drv, Vcc and HV throughout the netlist. This makes the netlist easier to read.
- Includes a Rich Text Format (RTF) Help Editor to make adding and linking help to models a snap.
- Link any netlist to a test drawing to show the model in action.

## Intusoft and SiSoft Join Forces with Partnership

SiSoft, a leading producer of signal integrity EDA tools, announced January 30th, 2004 that they have partnered with Intusoft. Intusoft has worked closely with SiSoft to provide the IsSpice4 simulation kernel as the heart of a new product series from SiSoft called, "Quantum-SI." The new product will be available in Q2 of this year and will provide leading signal integrity capability for much less than competitive offerings, and in cases with additional functionality. Quantum-SI was demonstrated and well received at this year's 2004 DesignCon tradeshow in Santa Clara, California.

SiSoft specializes in system-level signal integrity design and analysis of IC interfaces and electronic interconnects for deep-submicron ICs, advanced IC packages, connectors and cables in multi-chip/board configurations. More on SiSoft and its partnership with Intusoft can be found at: [www.sisoft.com](http://www.sisoft.com) and <http://www.sisoft.com/news04b.asp>.