AND8043/D

Implementing the SOFA in AC/DC Power Supplies

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APPLICATION NOTE

INTRODUCTION

The novel ON Semiconductor NCP1205 represents a real breakthrough in Switch Mode Power Supply (SMPS) controllers. By combining free–running operation and a Voltage Controlled Oscillator (VCO), the **S**oft **O**scillating **F**ree–running ch**A**rger or SOFA, allows true Quasi–Resonant (QR) or valley switching operation and soft frequency foldback when the output power demand diminishes. Implementing ON Semiconductor state–of–the–art Very High–Voltage Integrated Circuitry (VHVIC), the SOFA will naturally find a place in designs where soft–switching operation and ease of implementation are premium, as the following features emphasize:

- **Full Quasi–Resonant Operation:** By detecting the end of the transformer core demagnetization to initiate a new cycle, the SOFA ensures drain–source valley switching or QR operation. Furthermore, thanks a to comprehensive logic circuitry, the device jumps between the valleys as the built–in VCO starts to decrease the switching frequency. As a result, Electromagnetic–Interference (EMI) are reduced and turn–on losses are virtually null.
- **Voltage–Controlled Oscillator:** An internal VCO takes over as soon as the free–running frequency hits a maximum user adjustable value. As the output power demand further diminishes, the switching frequency is naturally reduced to ensure a better efficiency at light loads.
- **Low Standby–Power:** If SMPS naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand vanishes. By smoothly reducing the number of switching cycles per second, the SOFA drastically reduces the power wasted during light load conditions. In no–load conditions, the SOFA allows the total standby power to easily reach and exceed next International Energy Agency (IEA) recommendations.
- **Short–Circuit Protection:** By permanently monitoring the feedback line activity, the IC is able to detect the presence of a short–circuit, immediately reducing the output power for a total system protection. Once the short has disappeared, the controller resumes and goes back to normal operation. For given applications (e.g. constant output power supplies), you can easily disconnect this protective feature.
- **Over–Voltage Protection:** By continuously checking its own V_{cc} rail, the SOFA can safely go into permanent latch–off phase when the operating voltage exceeds 36 V. In Forward winding applications, this options lets you also protect the design against transient mains over voltages. For application where an adjustment is necessary, the SO–16 versions pins out the dedicated comparator input to let you select the protection level of your choice.
- **Large Supply Range:** Battery charger applications require that the controller can still control the output current when the output voltage is close to zero (e.g. a discharged battery). This is called Constant–Current/ Constant–Voltage (CC–CV) operation. To allow the controller self–supply when the output voltage disappears, one needs to wire the auxiliary winding in the Forward mode. However, most of today's primary side controllers have difficulty to cope with a Forward auxiliary winding operated on a universal mains because of the large voltage dynamics it implies. Fortunately, by authorizing 7.0 V through 36 V operation, the SOFA eases the designer task on the self–supply side.
- **Low Output Ripple in Standby:** Some loads are sensitive to the ripple present on the output. This is the case for Li–Ion batteries where a clean voltage is required to ensure the longest service. Standard hysteretic controllers produce unacceptable output ripple. By smoothly reducing the operating frequency, the SOFA generates a lower ripple when entering the standby mode.
- **No Acoustic Noise While Operating:** Instead of reducing the switching frequency at high peak currents, the SOFA waits until the peak current demand falls below a fixed $1/3^{rd}$ of the peak maximum limit. As a result, frequency reduction takes place without having a singing transformer … You can thus select cheap magnetic components free of noise problems.

January, 2001 – Rev. 0

Publication Order Number:
AND8043/D

- **External MOSFET Connection:** By leaving the external MOSFET external to the IC, you can select avalanche proof devices which, in certain cases (e.g. low output powers), let you work without an active clamping network. Also, by controlling the MOSFET gate signal flow, you have an option to slow down the device commutation, therefore reducing the amount of ElectroMagnetic Interference (EMI).
- **SPICE Model:** A dedicated model that lets you run transient cycle–by–cycle simulations is available to verify your theoretical design. Ready–to–use templates can be downloaded in OrCAD's PSpice, INTUSOFT's IsSpice and Spectrum–Software's μCap from ON Semiconductor web site, NCP1205 related section.

What is Valley Switching?

Figure 1 depicts a typical FLYBACK converter drain–source waveform. During the ON time, V_{ds} is close to zero, the power switch being closed. The input voltage is applied on the primary inductance Lp and the current ramps up with a slope of $\frac{V_{in}}{Lp}$ (eq. 1). When the controller dictates the switch opening (because of the Pulse Width Modulator or the peak current limit has been reached), the drain–source quickly rises and the energy transfer between primary and secondary takes place: the secondary diode conducts and the output voltage is also seen on the primary, over Lp. This plateau is equal to $V_{in} + N \cdot (V_{out} + V_f)$ where N is the secondary to primary turn ratio, V_{out} the output voltage and Vf the diode forward drop. During this time, the primary current decreases with a slope imposed by the reflected voltage $\frac{N \cdot (V_{out} + V_f)}{Lp}$ (eq. 2). Figure 2 zooms on the primary current, showing how it moves over one switching cycle.

When the primary current reaches zero, the transformer core is fully demagnetized: we are in Discontinuous Conduction Mode (DCM). The primary inductance Lp together with all the surrounding capacitive elements Clump create an LC filter. When the secondary diode stops conducting at Ip = 0, the drain branch is left floating since the MOSFET is already open. As a result, a natural oscillation takes place exhibiting the following frequency value: $Fring = \frac{1}{2 \cdot \pi \cdot \sqrt{Lp \cdot Clump}}$ (eq. 3) . As any sinusoidal signal, there are peaks and valleys. When you restart the switch in the valley, all the parasitic capacitor are at the lowest possible level and the capacitive losses $\frac{1}{2} \cdot Clump \cdot Vds \cdot Fsw$ (eq. 4) are kept small: the MOSFET is no longer the seat of turn–on losses and the usual turn–on parasitics are removed. Unfortunately, the perfidious leakage inductance degrades the beauty of Figure 1 and 2 by also ringing at the switch opening. The frequency is much higher than the natural frequency since L_{leak} is smaller than Lp. Care must be taken to not cheat the SOFA demagnetization block by this spurious signal.

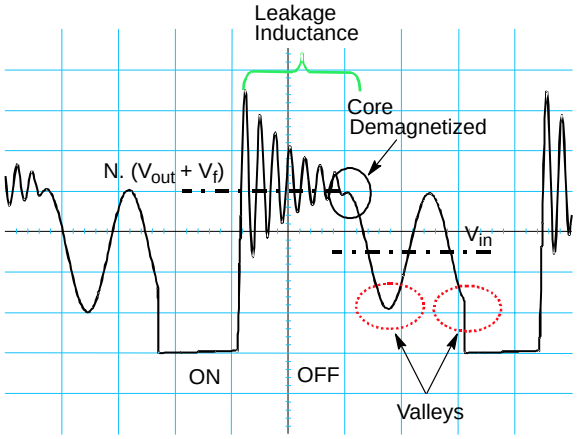

Figure 1. A Typical FLYBACK Drain–Source Waveform

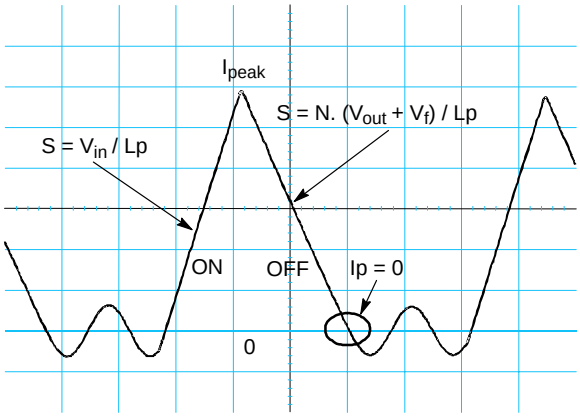

Figure 2. The Primary Current Ramps Up and Down to Zero in DCM

Observing the Core Flux

The core flux can easily be observed through an auxiliary winding wired as Figure 3 proposes:

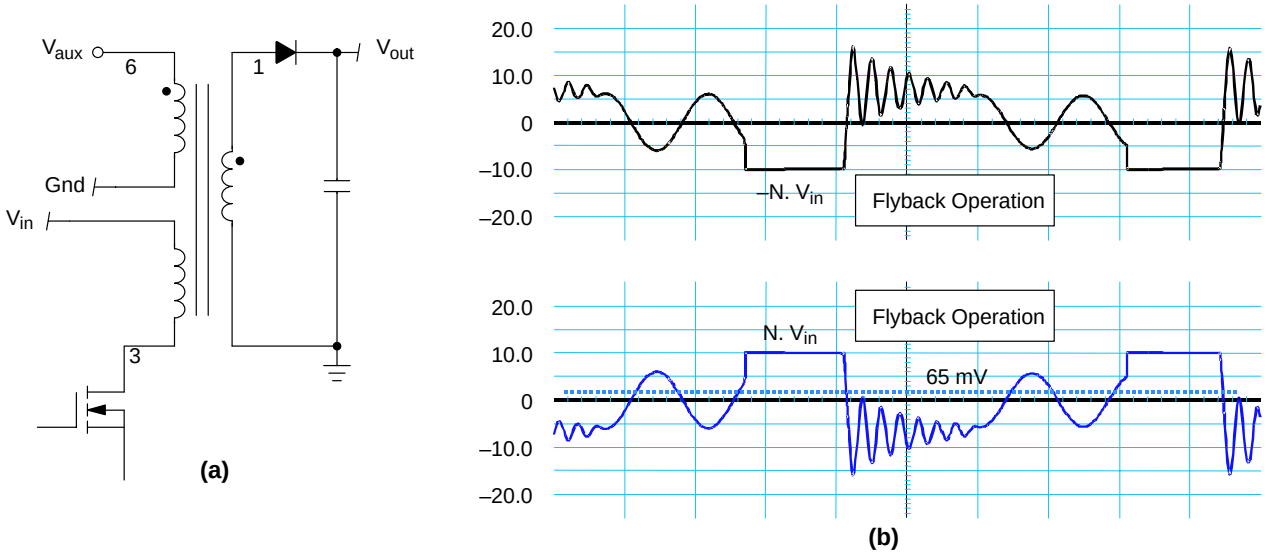

Figure 3. An auxiliary winding lets you observe the flux image in the transformer's core depending on the way you wire it: Flyback or Forward

Thanks to the coupling between the windings, the auxiliary section will deliver a voltage image of the core's flux through the following formula: $V_{aux} = N \cdot \frac{d\varphi}{dt}$ (eq. 5). Now, you can wire the winding either in Flyback (as the power winding) or in Forward. The observed signals look the same but the polarity is different as Figure 3b depicts. Please note that both signals are centered around the ground. We will see later on why battery chargers need Forward operation for a proper behavior. Figure 3b shows how a comparator featuring a reference DC level above ground can easily toggle up and down as soon as DCM occurs. The internal logic circuitry can then shape this signal to restart the power switch.

What is Free–Running Operation or SOPS Mode?

Self–Oscillating Power Supply (SOPS) or free–run operation portrays a power supply whose power switch is activated immediately further to the transformer's core demagnetization occurrence. The controller thus no longer needs an internal clock since external elements such as Lp, V_{out}, Ip etc. rule the operation. If a small delay is added further to the demagnetization comparator trip point, then the switch can be restarted right in the middle of the sinusoidal valley (See Figure 1). Let's see how we can describe the SOPS operation through the following equations:

$$t_{on} = \frac{Lp}{V_{inDC}} \cdot Ip \qquad \text{(eq. 6)}$$

$$t_{off} = \frac{Lp}{\left[\frac{Np}{Ns} \cdot (V_{out} + V_f)\right]} \cdot Ip \qquad \text{(eq. 7)}$$

$$t_{on} + t_{off} = Ip \cdot Lp \cdot \left[\frac{1}{V_{inDC}} + \frac{1}{\left[\frac{Np}{Ns} \cdot (V_{out} + V_f)\right]}\right] = \frac{1}{Fsw} \qquad \text{(eq. 8)}$$

$$P_{in} = \frac{P_{out}}{\eta} = \frac{1}{2} \cdot Lp \cdot Ip? \cdot Fsw \qquad \text{(eq. 9)}$$

$$\text{from eq. 9, } Ip = \sqrt{\frac{2 \cdot P_{out}}{\eta Lp \cdot Fsw}} \qquad \text{(eq. 10)}$$

Plugging (eq. 8) definition into the above equation (eq. 10):

$$Ip = \sqrt{\frac{\frac{2 \cdot P_{out}}{1}}{\eta \cdot Ip \cdot \left[\frac{1}{V_{in}} + \frac{1}{N \cdot (V_{out} + V_f)}\right]}} \qquad \text{(eq. 11)}$$

Solving for Ip

$$\rightarrow Ip = 2 \cdot P_{out} \cdot \frac{N \cdot (V_{out} + V_f) + V_{in}}{\eta \cdot V_{in} \cdot N \cdot (V_{out} + V_f)} \qquad \text{(eq. 12)}$$

Now extracting Fsw from eq. 10 and plugging it into eq. 8 leads to the switching frequency expression versus the output power:

$$Fsw = \frac{2 \cdot P_{out}}{\eta \cdot Lp \cdot \left(2 \cdot P_{out} \cdot \frac{N \cdot (V_{out} + V_f) + V_{in}}{(\eta \cdot (V_{in} \cdot (N \cdot (V_{out} + V_f))))}\right)^2} \qquad \text{(eq. 13)}$$

Feeding a math processor with eq. 13 and watching Fsw in the Y–axis while moving P_{out} shows how the switching frequency changes with power:

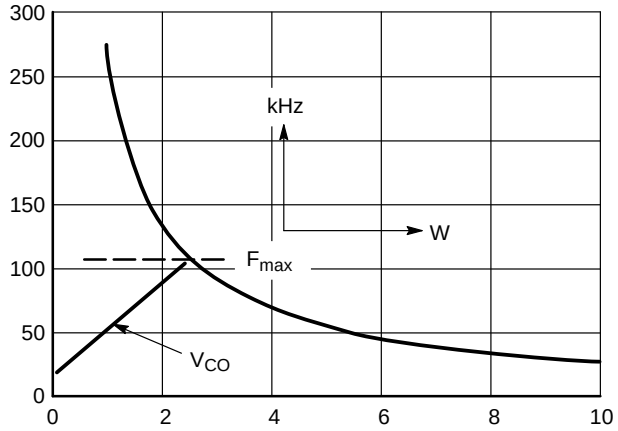

Figure 4. Switching Frequency Evolution with the Delivered Power (Lp = 6.0 mH, V_{in} = 120 VDC, N = 6.5)

As one can see, the switching frequency can grow in definitively if no clamping mean is provided. In the case of the SOFA, a VCO will smoothly reduce the switching frequency down to a few kilo–hertz as soon as the user selectable maximum frequency is hit.

Theory of Operation

As we have seen before, the SOFA combines free–running operation with minimum drain–source switching (so–called valley switching or quasi–resonant operation), which naturally reduces the peak current stress as well as the final EMI content at the switch closing. At nominal output power, the circuit implements a traditional current–mode SMPS whose peak current set point is given by the feedback signal. However, rather than keeping the switching frequency constant, each cycle is initiated by the end of the transformer core demagnetization. The system therefore operates at the boundary between Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM) while the switching frequency evolves with the operating conditions. Figure 5 details this terminology.

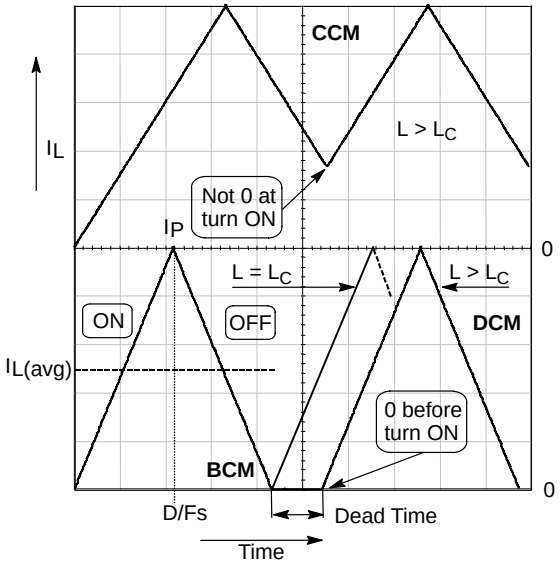

Figure 5. Depending on the primary current at turn–on, you can define various operating modes

When the output power demands decreases, the natural free–running switching frequency raises (Figure 4). As a natural result, switching losses also increase and degrade the SMPS efficiency. To overcome this problem, the maximum switching frequency of the NCP1205 is clamped to typically 125 kHz when a 1.0 nF capacitor is connected as the timing capacitor. As soon as the free running mode (also called Borderline Control Mode, BCM) reaches this clamp value, the internal VCO takes over and starts to decrease the switching frequency: we are in Variable Frequency Mode (VFM). Please note that during this transition phase, the peak current is not fixed but is still decreasing because the output power demand does. This ensures a very smooth transition between free–run and VFM modes. However, the frequency decrease is subordinate to the appearance of a valley as we have stated before: if the VCO dictates a switch restart, the logic latches the information until a valley is detected. Also, if the VCO timer would ask for a restart, the logic circuit will wait until the next valley level before giving the final green light. As a result, in VFM, discrete leaps between valleys occur and introduce a natural jitter: during these leaps, the peak current also toggle between different values to satisfy eq. 9 at every switching cycle. At a given state, the peak current reaches a minimum ceil (typically 250 mV/Rsense, eq. 14), and cannot go further down: the switching frequency continues its decrease down to a possible extremely low frequency. During normal free–running operation and VFM, the controller always ensures single drain–source valley switching. As soon as the VCO dictates a smaller switching frequency, the controller waits for the occurrence of the next valley before restarting the power switching.

To adjust the transmitted power, the PWM controller can play on the switching frequency or the peak current set point. To refine the control and thus offering a truly smooth transition between VCO and VFM operation, the NCP1205 offers the ability to play on both parameters either altogether or on an individual basis. In order to clarify the device behavior, we can distinguish the following operating phases:

- The load is at its nominal value, maximum output power. The SMPS operates in borderline conduction mode (BCM) and the switching frequency is imposed by the external elements (V_{in}, Lp, Ip, V_{out}). The MOSFET is turned on at the minimum drain–source level. The peak current is controlled via the feedback voltage (V_{FB}) which undergoes an internal inversion: if V_{FB} goes up → Ip goes down and vice versa.
- The load starts to decrease and, as a natural consequence, the free–running frequency increases until it hits the maximum level externally set by the timing capacitor. At this time, the VCO takes over the loop control and tries to force a frequency decrease. However, since the internal logic has no other options than accepting valley transition only, a second valley switching takes place. As the power further decreases, the population of second valleys increases. The peak current jumps between Ip1 and Ip2 to cope with the discrete frequency transitions within the cycles: one valley gives Fsw1 and Ip1 adjusts to satisfy eq. 9, while two valleys give a lower frequency and Ip2 rises during this event, always to satisfy eq. 9.
- At a certain moment where Pout has further diminished, there are only two–valley switching events and a stable condition takes place. Ip has no other option than going down, until it is frozen at the very minimum ceil: 250 mV/Rsense.
- The VCO now controls the switching frequency with fixed current pulses. Fswitching diminishes while other valley jumps take place. Figure 6 shows a typical frequency versus power graph for a low power charger (Pnominal = 5.0 W).

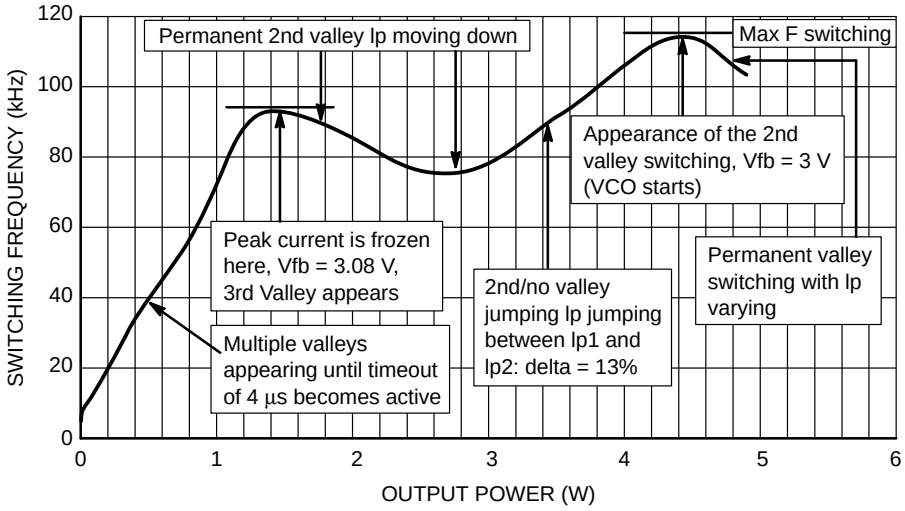

Figure 6. This Graph Shows how the Frequency and Current Move until the Current is Frozen

Figure 7 depicts how the waves were captured to plot Figure 6 graph. The output current (V_{out} = constant) was reduced and the drain–source signal was observed then memorized.

Figure 7. Multiple pulses start to occur further to the transition into VCO control

The Decaying Sine Wave

The drain–source wave has a sinusoidal shape exponentially amortized over time. The decay is dependent upon the ohmic losses of the equivalent Lp . Clump composing the ringing circuit. As a matter of fact, the case quickly arises that no more valleys are available to trigger the internal SOFA circuitry when the VCO has lowered the frequency. To circumvent this problem, the device implements a timeout (*timo*) which is reset at each valley occurrence. If the next valley does not appear within a time window of 4.0 μs, then the timeout gives the authorization to restart but the SOFA waits for the VCO clock appearance before actually driving the power MOSFET. Figure 8 portrays different states showing how the pulses evolve with power and how the *timo* automatically initiates a new cycle at the end of the decay period:

Figure 8. Typical operating waveforms for different output powers down to no–load operation (bottom curve)

Advantages of the Method

By implementing the aforementioned control scheme, the SOFA brings the following advantages:

1. Discontinuous only operation: in DCM, the FLYBACK is a first order system (at low frequencies) and thus naturally eases the feedback loop compensation.
2. A low–cost secondary rectifier can be used thanks to soft blocking conditions (Ip goes down to zero and the diode stops conducting, unlike in CCM where the power switch turn–on event forces the diode to brutally stop conducting).
3. Valley switching ensures minimum switching losses brought by Coss and all the parasitic capacitances.
4. By folding back the switching frequency, you turn the system into Pulse Duration Modulation. This method prevents from generating *uncontrolled* output ripple as with hysteretic controllers.
5. By letting you control the peak current value at which the frequency goes down, you ensure that this level is low enough to avoid transformer acoustic noise generation even at audible frequencies.

Feedback, Current Set Point and Error Circuitry

The feedback voltage (FB pin) undergoes an internal inversion before imposing the final current set point. This is shown on Figure 9. As you can see, the error amplifier output expression is: $Verr = 10 - 3 \cdot V_{FB}$ using the resistor values as given on the schematic. The error signal is then divided by three (to offer a sufficient dynamic on the FB pin) and is classically clamped to 1.0 V. Now, if you carefully look at Figure 9, you notice the presence of a diode and 250 mV reference. The presence of these two elements prevents the peak current to go below 250 mV/Rsense, Rsense being the external power sense resistor. As a result, the peak current can only move between 1.0 V/Rsense and 250 mV/Rsense. When the 250 mV clamp is activated, it means that the VCO has already taken the lead of the SMPS. This is depicted by Figure 10 sketch where you can see the current set point evolution.

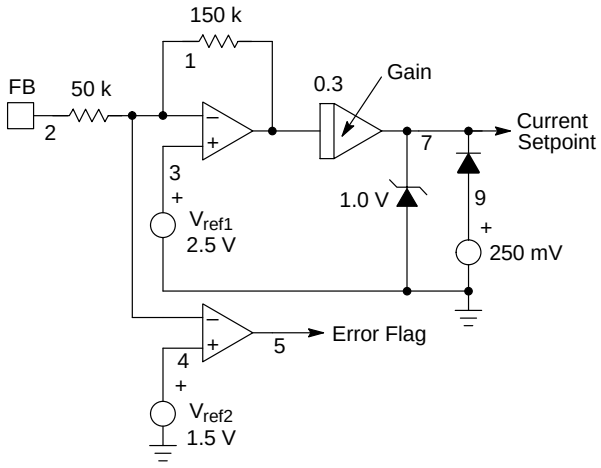

Figure 9. This component arrangement lets you monitor the (+) signal and detect when it leaves its limits

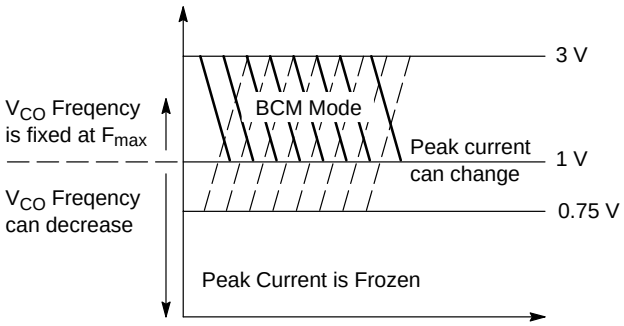

Figure 10. The current is frozen below a given limit and cannot go further down

Actually, the SOFA features an internal error amplifier solely used to detect an over current problem (OCP). The internal error amplifier is used to create a virtual ground permanently biased at 2.5 V, an internal reference level. By monitoring this virtual ground further called V(–), we have the possibility to confirm the good behavior of the loop. If by any mean the loop is broken (shorted optocoupler, open LED etc.) or the regulation cannot be reached (true output short–circuit), the OPAMP network is adjusted in order to no longer be able to ensure the 2.5 V virtual point V(–). If V(–) passes down the 1.5 V level (e.g. output shorted) for a time longer than 128 ms, then the pulses are stopped for 8 x 128 ms. The controller enters a kind of burst mode with bunch of pulses lasting 128 ms (typical with Ct = 1.0 nF) and repeating every 8 x 128 ms. If the loop is restored within the 8 x 128 ms period, then the pulses are back again on the output drive (synchronized with $UVLO_H$). Figure 11 depicts a scope shot of the drain–source pulses in presence of a short:

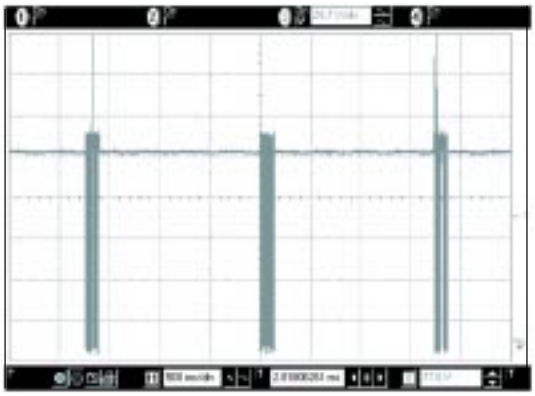

Figure 11. In presence of a short, the SOFA enters a controlled burst mode to keep the power dissipation within safe limits.

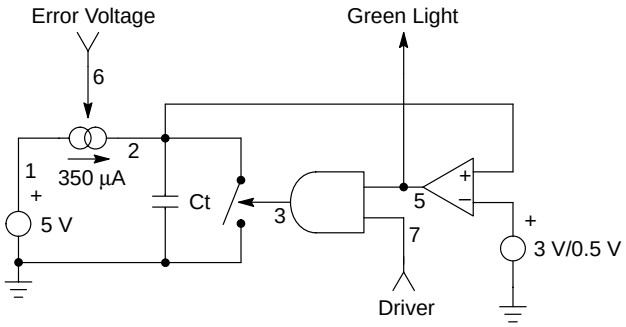

Figure 12. This picture details the oscillator section

Frequency Management

As we have detailed, the power switch restart is initiated when two information are present: the core demagnetization has occurred and the internal timer validates it. The VCO simplified circuitry is shown on Figure 12. In free–run operation, the timer capacitor is charged at the highest rate (≈ 350 μA) and is transparent to the circuit: it always gives the green light before the core's demagnetization signal happens. The capacitor timer signal thus ramps up to 5.0 V and stays there until it is discharged by the driver signal. During free–run operation, the error voltage controlling the 350 μA current source (in fact that is a voltage–controlled current source) is clamped to 1.0 V. As soon as the internal feedback voltage (the error amplifier output) goes below 1.0 V, then the charging current obeys the law Icharge = Verror x 350 μA, down from 350 μA (Verror = 1.0 V) to nearly zero (Verror ≈ 0). The switching frequency at a given Ct is thus calculated knowing the capacitor swing (500 mV to 3.0 V) and the maximum charging current of 350 μA:

$$\Delta t = Ct \cdot \frac{\Delta V}{350\ \mu A} \text{ or } 130\ kHz\ @\ Ct = 1.0\ nF \quad \text{(eq. 15)},$$

including a total 500 ns discharge time. In practice, accounting for the internal element precisions, a 110 kHz is typically given in the data–sheet. Figure 13 gives the typical frequency versus the feedback pin level shape for the SOFA. The frequency starts to decrease when Vfb is around 3.1 V.

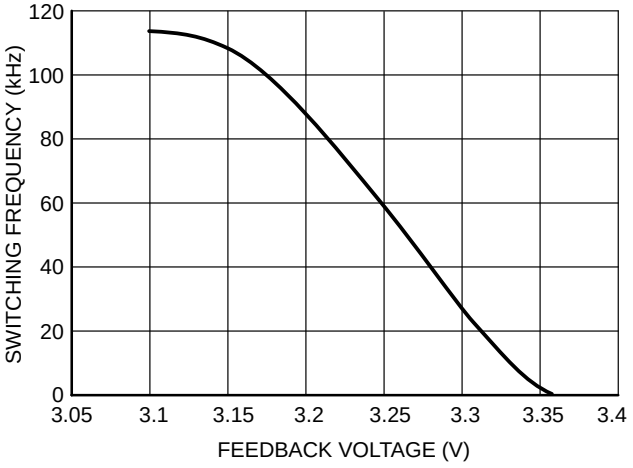

Figure 13. The VCO versus feedback voltage transfer function (Ct = 1.0 nF)

In VCO mode (also called VFM), the charging current diminishes and Ct reaching 3.0 V gives the VCO green light. However, the power switch will effectively be driven high only when both Ct and demagnetization end both give the green light. This is important to respect the multiple wave jumps. Figure 14 and 15 detail Ct signals at two different points: free–run and VFM.

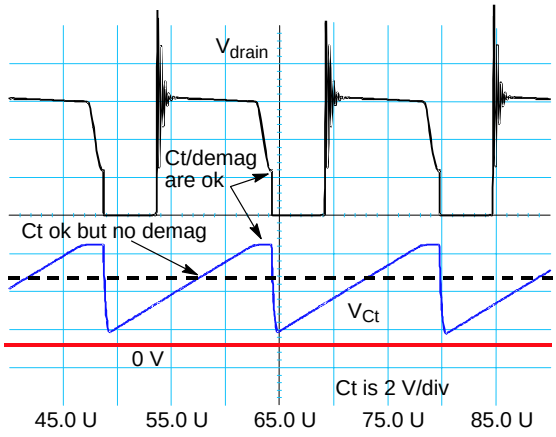

Figure 14. Free–run operation: Ct is okay to restart but the demagnetization signal is not yet arrived . . .

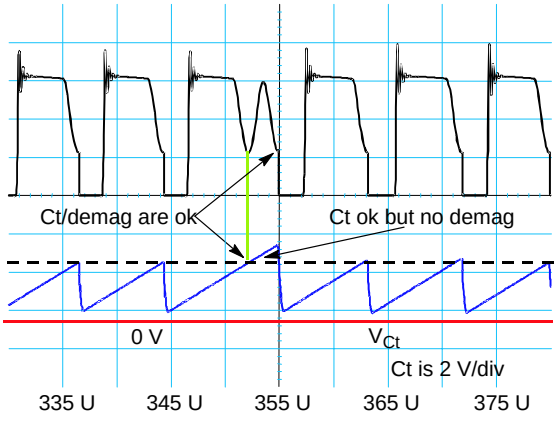

Figure 15. Here, we are in VFM and Ct rules the operation. Sometimes Ct says okay but, again, the demagnetization has not arrived: next wave is fine.

Design Rule The SOFA operates in free–run until the frequency increases (Pout diminishes) and the VCO starts to clamp then folds the frequency back. Always keep a 20% difference between the maximum frequency imposed by the VCO (through Ct) and the frequency occurring at maximum power in free–run operation (eq. 16). If this condition is not respected, there are chances that the regulation is lost at the highest output level. As an example, if the maximum switching frequency is selected to be 90 kHz, then the maximum output power shall be reached at a frequency less or equal than 70 kHz.

Fault Management

As we saw before, the SOFA hosts a dedicated timing circuitry only activated during the presence of a short–circuit. As soon as the 2.5 V virtual ground is lost (Figure 9), Ct is routed to a fixed charge/discharge current generator which produces an internal 1.0 kHz frequency (Ct = 1.0 nF). This 1.0 kHz is internally divided to produce a 128 ms timeout. If the short circuit lasts more than 128 ms, then the output pulses are permanently stopped for a complete 8 x 128 ms or 1 second (Ct = 1.0 nF). During this time, Vcc goes up and down. Once this period is elapsed, the SOFA resumes and attempts to restart. If it cannot (because the short is still there), then a new 128 ms cycle takes place. Please note that Ct being routed to the timeout generator, the SOFA enters the free–un operation in error mode.

Design Rule The power supply start–up period (when you plug the system into the wall until it actually regulates) shall last less than 128 ms (if Ct = 1.0 nF) otherwise a short–circuit like situation will occur and the supply will fail to crank. Also, please note that the fault timer circuitry is not synchronized with the Vcc level. As a result, the 128 ms burst can only appear on the drive output for a going down Vcc (15 to 8.0) and not during a going up Vcc (8.0 to 15) where the pulses are automatically invalidated (as with a startup sequence). Because of this lack of synchronization, the 128 ms burst can sometimes be truncated if it starts in the Vcc ramp–up portion. This is not a problem in the application:

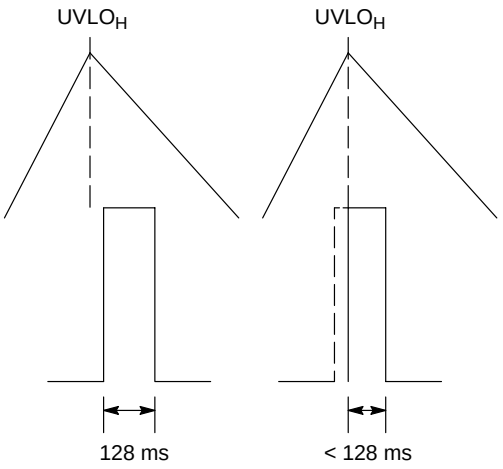

Figure 16. The burst can be truncated when it occurs before $UVLO_H$

Startup Section

The SOFA includes a 3.0 mA startup current source directly connected to the mains. It is capable to permanently sustain up to 500 V without a problem. During the startup sequence, the 3.0 mA charges the V_{cc} capacitor. Once $UVLO_H$ has been reached, the error timer circuitry is triggered because the supply output voltage does not regulate V_{out}. After startup, providing the self–supply is present, the current source is turned off, dissipating very few mW. Figure 17 portrays a typical startup sequence:

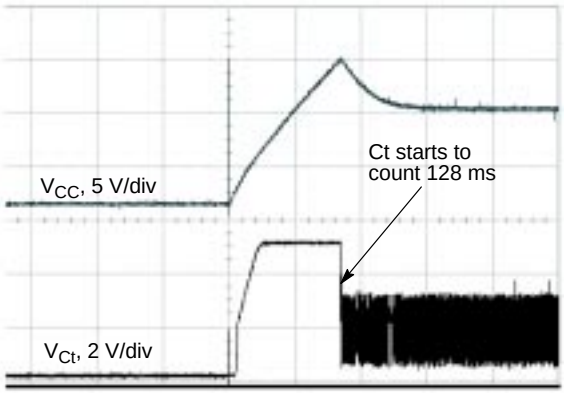

Figure 17. A typical startup sequence showing Ct activity at $UVLO_H$

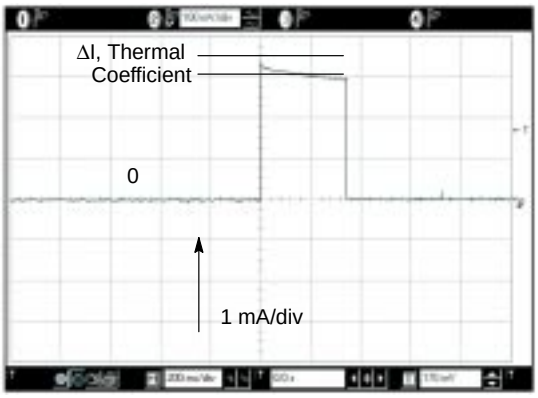

Figure 18. A typical startup shape illustrating the thermal coefficient on the current source (1.0 mA/div)

As Figure 18 depicts, a thermal coefficient is naturally present on the high–voltage startup current source. Because the die heats up, the current set point is modified to slowly reduce the current delivered to the Vcc capacitor.

Demagnetization Circuit and Auxiliary Winding

The demagnetization portion plays an important role in the SOFA application. Its role consists in monitoring the transformer core activity and restart the power switch once the core reset has occurred. This function is accomplished by checking the level on a dedicated auxiliary winding as portrayed by Figure 19:

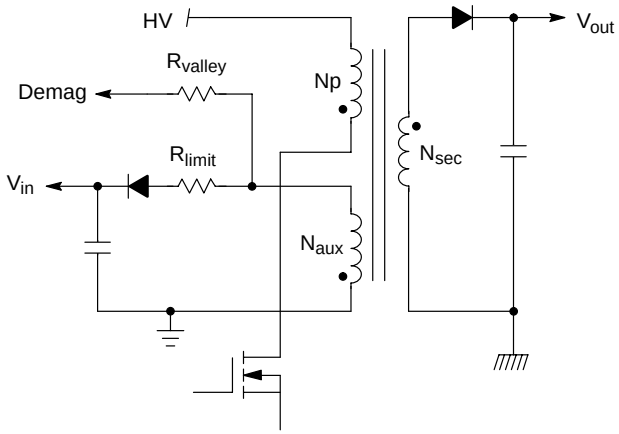

Figure 19. Implementing the demagnetization with the auxiliary supply wired in Forward mode

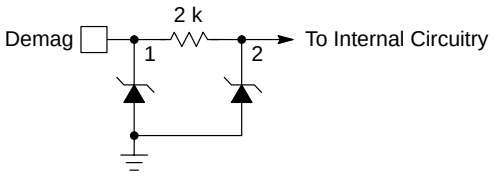

Figure 20. The front ESD zener diode exhibits a parasitic capacitance of roughly 10 pF

Rvalley limits the maximum current flowing through the SOFA demagnetization pin (≈ 3.0 mA is a good value) but also forms a delay network when combined with the pin input capacitance (10 pF typical at low voltages thanks to ESD protection network, Figure 20). Once the power supply prototype has been built, a few tweak on Rvalley will let you find the right value to restart right in the minimum drain valley (Figure 21):

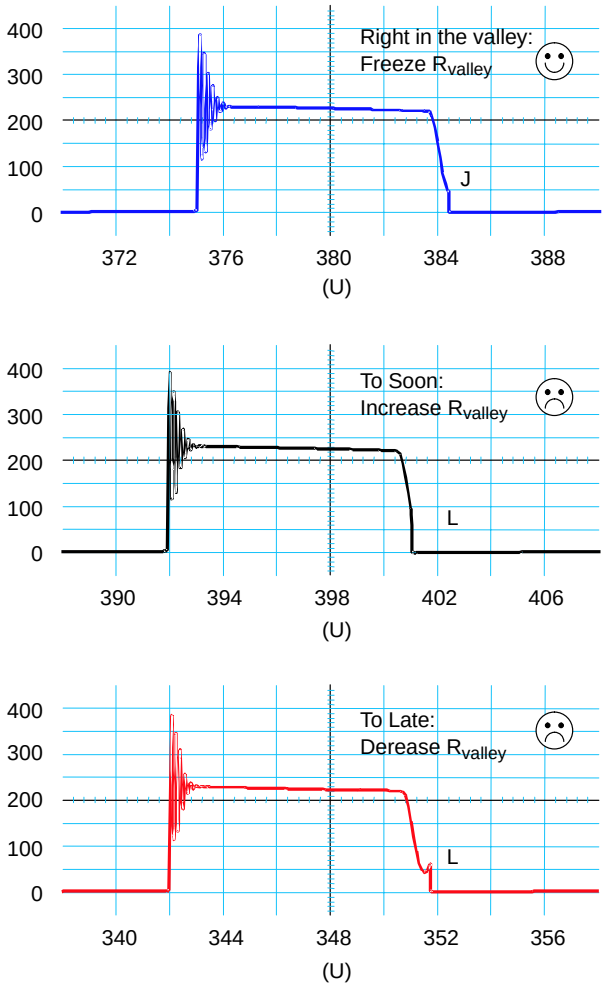

Figure 21. A tweak on Rvalley allows to restart right in the middle of the wave

Since we are operating the winding in Forward, it behaves as a low impedance voltage source. A resistor is thus required to limit the maximum peak current flowing through the Vcc capacitor but also through the auxiliary diode (typically a 1N4148 can do the job).

The SOFA has been designed to accept a demagnetization polarity corresponding to an auxiliary winding operated in the Forward mode (dot position on Figure 19 and Figure 3b signals). The Aux Vcc node will thus be at a level equal to: $Vcc = VHV \cdot \frac{Naux}{Np}$. This is true when the duty–cycle is large enough (e.g. at a nominal load level). When the load goes down, the duty–cycle also diminishes until the peak current is frozen (≈ 250 mV/Rsense). The Vcc is therefore affected by a ripple depending on the amount of charge you bring in (during the ON time) and the amount of charge delivered to the load (the SOFA IC). You thus need to check that the Vcc stays at a minimum of 8.0 V at any load and mains conditions but also remains lower than the maximum allowable Vcc to not shut down the IC (highest mains and maximum output current). We will tackle this point in the design example.

In some applications, where you need to implement a precise overvoltage protection, an auxiliary self–supply configured in Flyback is mandatory to offer a primary image of what is going on the secondary. To still allow the demagnetization detection, Figure 22 proposes a solution built around two extra diodes and one resistor.

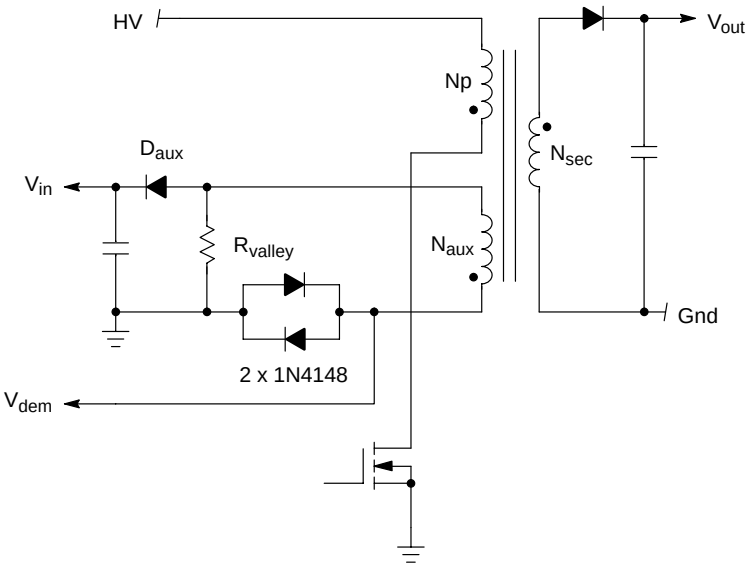

Figure 22. A simple component arrangement allows a detection in Flyback mode

During the ON time, the Demag point goes high but clamp to one Vf. The auxiliary diode being blocked, Rvalley closes the path to ground and fixes the output impedance. You can thus directly drive the demagnetization pin from this point, Rvalley inserting the same delay as on Figure 19. At the switch opening, the auxiliary voltage also reverses and the other diode ensures a Demag level of –Vf. When DCM occurs, the Demag line crosses the 65 mV threshold and reactivates the SOFA circuitry.

The Perfidious Leakage Inductance…

As usual, the leakage inductance will bother the designer but this time not in the sense of a lethal kick but rather because of its high frequency nature. The SOFA demagnetization circuitry features a threshold of typically 65 mV which is very sensitive. If the leakage inductance is high and the reflected voltage low, e.g. during power up, then there are chances that the leakage inductance ringing is internally interpreted as a demagnetization signal and the SOFA will restart the switch: you enter CCM and the switching frequency becomes very high, implying a possible MOSFET over dissipation. Figure 23 shows how the problem takes place:

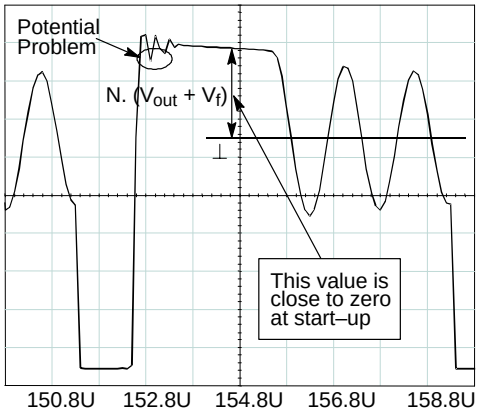

Figure 23. Potential problems can arise from an energetic leakage effect (Spice simulation)

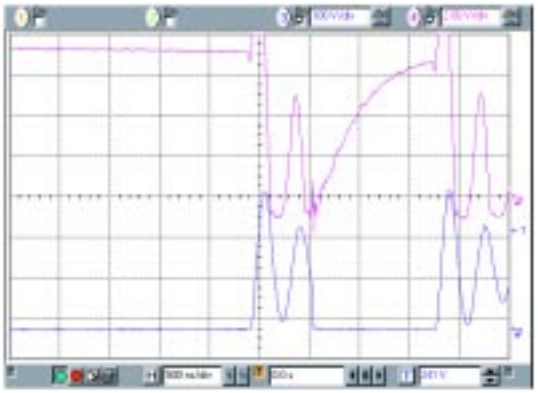

Figure 24. Multiple high frequency restart occurs because of the leakage

At the very beginning, just when $UVLO_H$ is crossed by the Vcc line, the first pulse takes place. Because V_{out} is down to zero, you only reflect (N x Vf) which can be pretty low, especially with a Schottky diode. As a result, the leakage ringing can be so strong (the peak current set point is pushed into its upper stops) that it crosses the V_{in} reference level (or the ground on the auxiliary winding, Figure 23) and triggers the demagnetization comparator. In normal operation, it could not append because the internal timer clamps the maximum switching frequency to Fsw max = 110 kHz. Unfortunately, at start–up, the timer is routed to the fault detection circuitry and does not plays its usual clamping role and total free–run is authorized. Pulses appear at a very high recurrent frequency until V_{out} starts to be significant and elevates the leakage inductance floor. At this time, the demagnetization Zero Crossing Detector (ZCD) is no longer bothered by this default. Figure 24 shows the true behavior of an application board without any damping network. The drain (lower trace) is close to the ground and the leakage ringing restarts the SOFA controller. The switching frequency is very high…

A possible cure consists in further integrating the ZCD signal with an additional capacitor wired between the feedback pin and ground. This option adds another delay and the true valley switching can be lost. Another option takes the form of an R–C damper wired on the transformer primary. Trials will be necessary to find a balance between the damping effect and a reasonable efficiency degradation.

The Driving Stage

As we have seen, the SOFA sustains operating voltages up to 35 V. Obviously, the driving level delivered by the circuit cannot be that high, otherwise the power MOSFET gate–source oxide would immediately be destroyed. The SOFA features a patented non–dissipative driving stage which clamps the Vgs to 12 V but offers a boost at low Vcc levels. Because the driver behaves like a voltage source (unlike a true current source with bipolar output stages), the rising edge of the signal can be the seat of a short ringing wave which occurs at the Miller transition. This pulse occurrence is normal and gets higher as the driver clamps more heavily. It does not have any effect the supply operation:

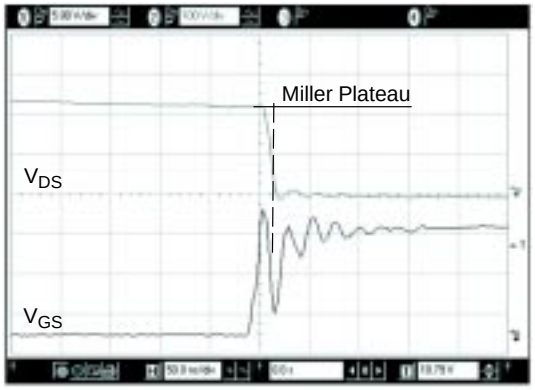

Figure 25. A small glitch occurs at the Miller transition

The SOFA Vcc operating range being quite large, always check that the selected power MOSFET accepts Vgs down to 6.0 V. A logic threshold device is recommended in case of extended operation close to $UVLO_{LOW}$ (6.5 V min).

The decaying plateau on the top of the Vgs signal is due to the internal bootstrap capacitor that slowly discharges during the transition.

Overvoltage Protection

The SOFA offers two types of overvoltage protection (OVP): one through the Vcc pin and another one via a dedicated pin only available on the DIP14 package.

Figure 26 depicts the internal implementation which reveals the presence of several zener diodes connected in series. The DIP14 offers a direct access to the comparator input for a different OVP level selection. The typical threshold level is stated at 2.5 V. With a 20 kΩ input impedance, we recommend the use of a zener diode as proposed by Figure 27. A capacitor can be added in very noisy environments. Final OVP level is thus Vz + 2.5 V.

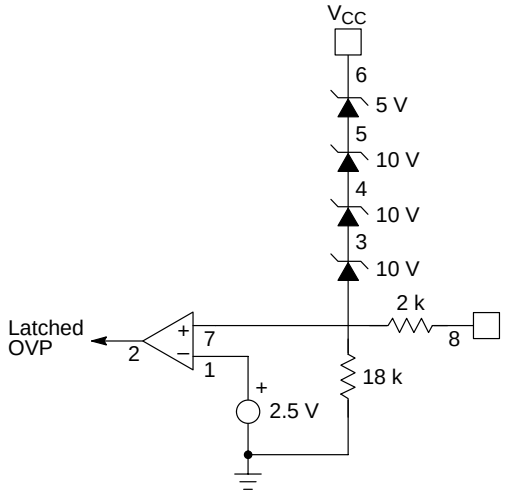

Figure 26. The OVP is made with four 10 V zener diodes connected in series

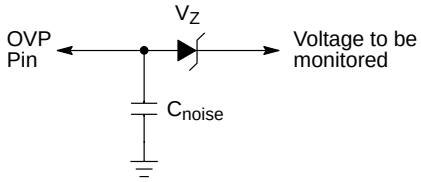

Figure 27. A possible OVP implementation with the DIP14 version

A Design Example

Now that we went through the description of the internal SOFA blocks, we will detail how to calculate the main components and particularly the transformer. The specifications are the following and correspond to a generic power supply application:

V_{in}: 90 to 250 VAC
V_{inDC} min = 120 V
V_{inDC} max = 350 V
P_{out} = 10 W
V_{out} = 6.5 V → I_{outDC} = 1.53 A, R_{load} = 4.2 Ω
Target efficiency = 80%

For EMI reasons, we want to keep Fmax below 90 kHz. The maximum power in free–run shall thus take place at 90–20% = 70 kHz. Now, as eq. 12 shows, we need several elements to compute our primary peak current defined by: $Ip = 2 \cdot Pout \cdot \frac{N \cdot (Vout + Vf) + Vin}{\eta \cdot Vin \cdot N \cdot (Vout + Vf)}$. Worse case appears at nominal output power and lowest input line level (120 VDC): Ip is the highest and Fswitching the lowest.

Turn Ratio Calculation

The turn ratio N fixes the level of Ip but also the type of secondary diode you will select. It actually affects several parameters:

- The drain plateau voltage during the OFF time: the lowest plateau gives room for the leakage inductance spike before reaching the MOSFET's BVdss: $Vplateau = \frac{Np}{Ns} \cdot (Vout + Vf) + VinDC_{max}$ (eq. 17).
- The secondary Peak Inverse Voltage (PIV) is linked to the turn ratio and the regulated output voltage by: $PIV = \frac{Ns}{Np} \cdot VinDC_{max} + Vout$ (eq. 18). If you lower the plateau voltage, you will increase the reverse voltage the secondary diode must sustain.
- The amp–turns equation $Np \cdot \alpha Ip = Ns \cdot Is$ should satisfy the average output current demand with $Iout_{avg} = \frac{Ip \cdot toff \cdot Fsw \cdot \alpha}{2 \cdot \frac{Np}{Ns}}$ (eq. 19). The α parameter illustrates the energy diverted by the leakage inductance at the switch opening (take 0.95 for low leakage designs).

With these numbers in mind, you can tweak the turn ratio according to the MOSFET BVdss and the diode. Below are given ON Semiconductor references for Schottky diodes:

Reference	V_{RRM} (V)	Io (A)	Case
MBRM120LT3	20	1	PowerMite
MBRM130LT3	30	1	PowerMite
MBRA130LT3	30	1	SMA
MBRA140LT3	40	1	SMA
MBRS120LT3	20	1	SMB
MBRS130LT3	30	1	SMB
MBRS140LT3	40	1	SMB
MBRS190T3	90	1	SMB
MBRS1100T3	100	1	SMB
MBRS320T3	20	3	SMC
MBRS330T3	30	3	SMC
MBRS340T3	40	3	SMC
MBRS360T3	60	3	SMC
1N5817	20	1	Axial
1N5818	30	1	Axial
1N5819	40	1	Axial

Please see brochure BR1487/D for thermal and package details.

If we select an MBRS340T3 (V_{RRM} = 40 V), then the PIV should be selected around 35 V at high line: $N = \frac{PIV - Vout}{VinDC_{max}}$ (eq. 20). If we select Np:Ns = 1: 0.08, then PIV = 28 V at 350 VDC input voltage which is okay with the selected diode. The plateau voltage at the drain will establish around 430 VDC: it leaves up to 170 V for the leakage spike with a 600 V MOSFET transistor.

The average diode Id_{avg} current is the converter's DC output current which is 1.5 A, in line with our 3.0 A MBRS340T3.

Primary Inductance

Plugging N into eq. 12 gives a peak current of 482 mA. We should now select the primary inductance to cope with our 70 kHz requirement. A simple spreadsheet plotting $Y = \frac{2 \cdot Pout}{\eta \cdot Lp \cdot Ip^2}$ while displaying incremental values for Lp in the X–axis will offer a possible selection for the primary inductance:

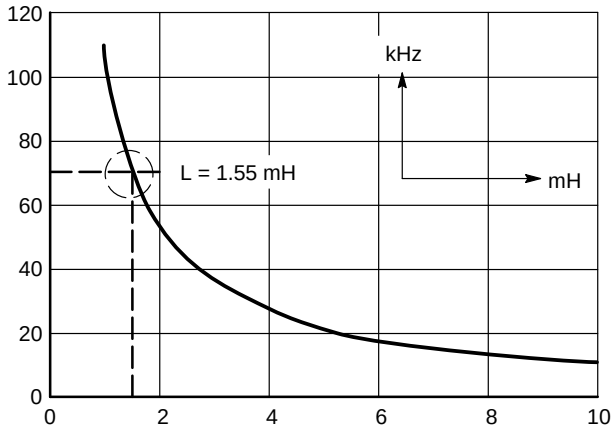

Figure 28. A graph plotting Fsw versus Lp offers a fast selection process

A 70 kHz operating frequency is obtained with a primary inductance of $\frac{2 \cdot Pout}{\eta \cdot 70 \cdot 10^3 \cdot Ip?}$ = 1.55 mH. In the lower SOFA limit (0.9 V), we need to be able to develop our peak current target of 480 mA. The minimum shunt value is therefore: 0.9/0.48 = 1.87 Ω. Let's pick–up an 1.8 Ω normalized value. This shunt being affected by a ±5.0% tolerance, the new worse case reveals a maximum peak of 1.1/1.71 = 643 mA. Furthermore, we need to account for the maximum SOFA propagation delay (250 ns) which, together with the primary slope, affects the final value. Worse case arises at the highest line: $\frac{350 \cdot 250\,n}{1.55\,m}$ = 56 mA. The total maximum peak current can thus be: 643 mA + 56 mA = 699 mA.

The basic transformer specs are therefore:

Lp = 1.55 mH
Np : Ns = 1 : 0.08
Maximum peak current = 691 mA

To verify our design, we can plug our numbers into a SPICE simulator using the transient SOFA model. The below schematic exemplifies the INTUSOFT's IsSpice4 model where the components have been assigned with the calculated values:

Idrain RMS = Iprimary RMS = 182 mA
Idiode secondary RMS = 2.53 A, Iavg = Iout
Fswitching = 64 kHz

The above values let you evaluate the MOSFET conduction losses (Pcond = Rdson @ Tj = 100°C x I_drain RMS), the secondary diode conduction losses (Pcond = Vf x Iavg + Rd x I_diode RMS). The primary/secondary RMS currents will determine the wire size when designing your transformer.

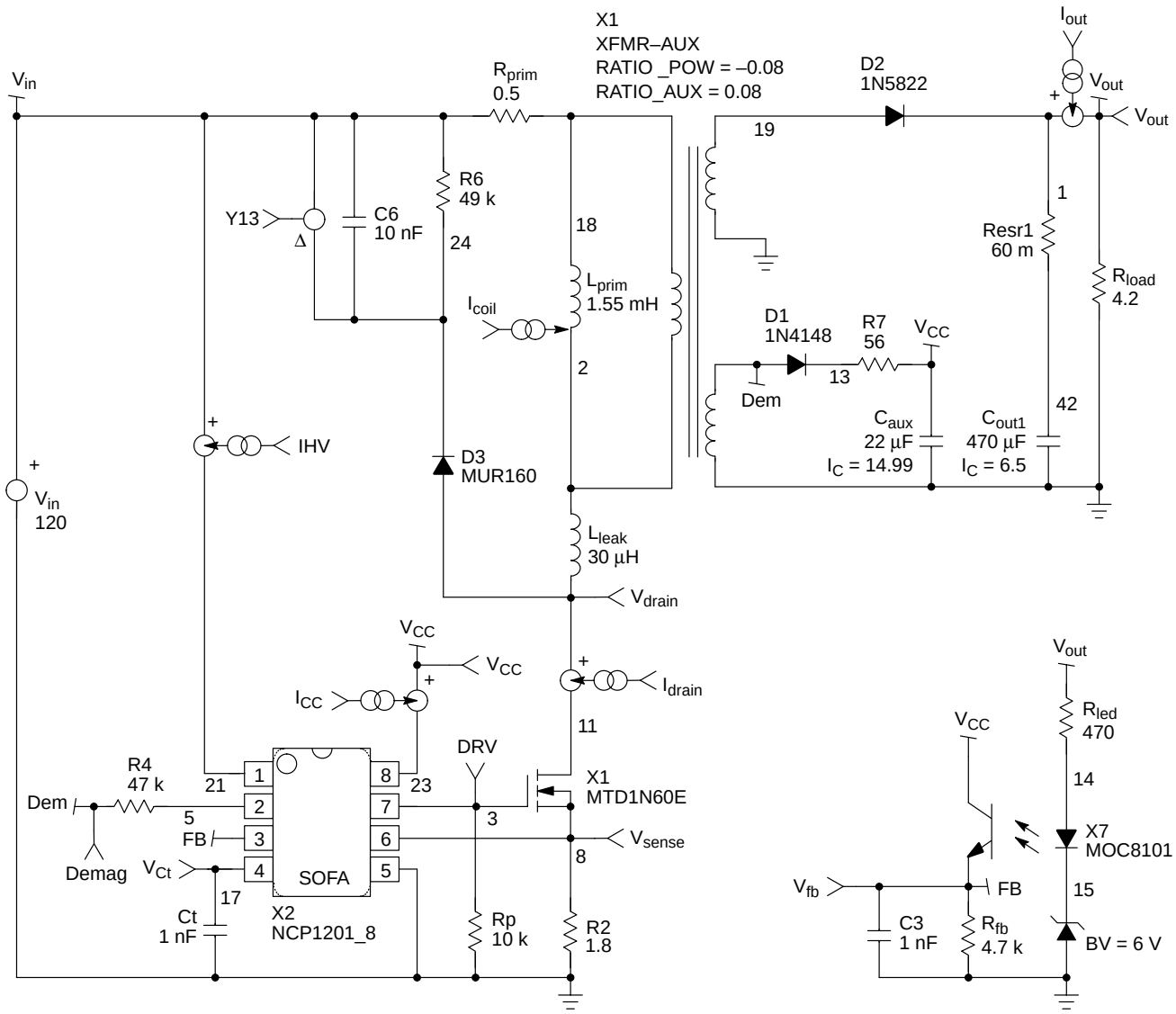

Figure 29. A Typical SPICE Simulation Testing the Design Validity

The following curves give you the most important wave shapes and let you deduct the other design parameters:

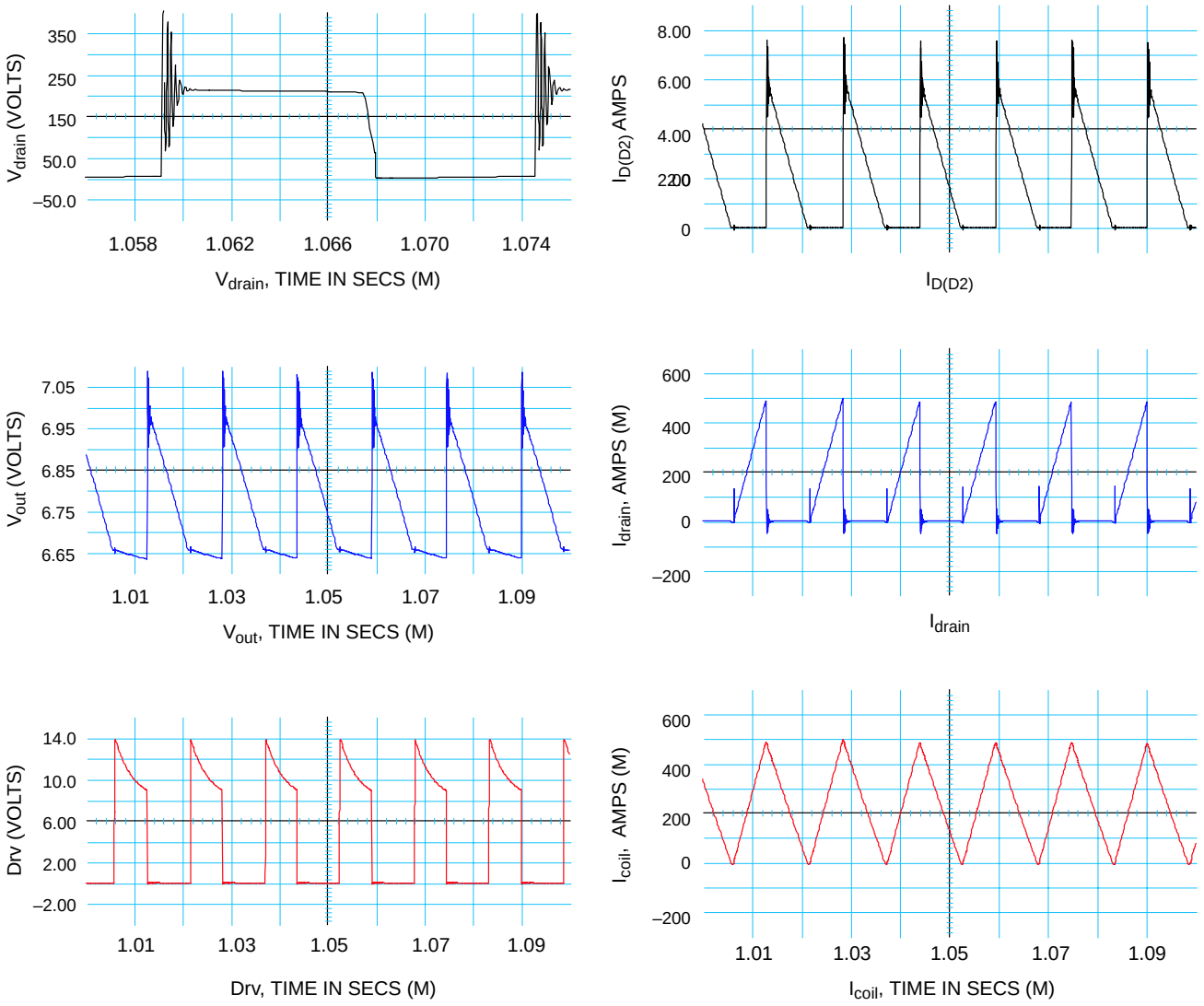

Figure 30. Various Simulation Results Revealing Important Values

Protecting the Power MOSFET

If the leakage inductance is kept low, an avalanche rugged MOSFET such as the MTD1N60E can withstand *accidental* avalanche energy, e.g. during a high–voltage spike superimposed over the mains, without the help of a clamping network. However, if this leakage path permanently forces a drain–source voltage above the MOSFET BVdss (e.g. 600 V), a clamping network is mandatory and must be built around a passive RC network or a Transient Voltage Suppressor (TVS). Figure 31 depicts the phenomenon while the below lines details the calculation steps:

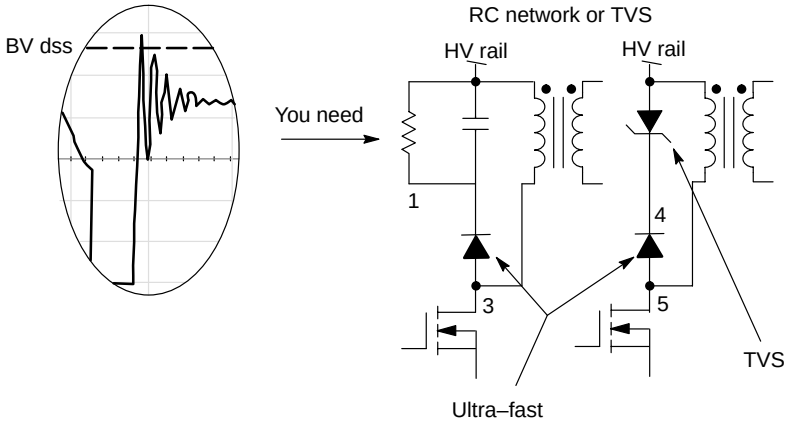

Figure 31. Care must be taken to ensure a safe operation of the MOSFET

1. RCD Network

The RCD network will permanently impose a fixed clamping level that will oppose to the leakage voltage. As a result, the drain will be clamp to V_{HVrail} + Vclamp. You normally select a clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

To calculate the component values, the following formulae will help you:

$$Rclamp = \frac{2 \cdot Vclamp \cdot (Vclamp - (Vout + Vf\,sec) \cdot N)}{Lleak \cdot Ip? \cdot Fsw} \quad \text{(eq. 21)}$$

$$Cclamp = \frac{Vclamp}{Vripple \cdot Fsw \cdot Rclamp} \quad \text{(eq. 22)}$$

The power dissipated by Rclamp can also be expressed by:

$$P_{Rclamp} = \frac{1}{2} \cdot Lleak \cdot Ip? \cdot Fsw \cdot \frac{\frac{Vclamp}{(Vout + Vf\,sec) \cdot N}}{\frac{Vclamp}{(Vout + Vf\,sec) \cdot N}} - 1 \quad \text{(eq. 23)}$$

with:

Vclamp: the desired clamping level

Ip: the maximum peak current (e.g. during overload)

V_{out} + Vf: the regulated output voltage level + the secondary diode voltage drop

Lleak: the primary leakage inductance

N: the Ns:Np conversion ratio

Fsw: the switching frequency

Vripple: the clamping ripple, could be around 20 V

Our 10 W power supply imposes Rclamp = 49 kΩ/1.0 W Cclamp = 10 nF D = MUR160 from ON Semiconductor

2. Transient Voltage Suppressor

Despite the low–cost offered by the above RC solution, the clamping level unfortunately varies with the peak current. If you need a very precise clamping level, you must implement a zener diode or a TVS. There are little technology differences behind a standard zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of zener. A 5.0 W zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5.0 W of continuous power but is able to accept surges up to 600 W @ 1.0 ms. If the peak power is really high, then turn to a 1.5KE200 which accepts up to 1.5 kW @ 1.0 ms.

Select the zener or TVS clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

3. Snubber Network

Another option lies in implementing a snubber network which will damp the leakage oscillations but also provide more capacitance at the MOSFET's turn–off. The peak voltage at which the leakage forces the drain is calculated by: $Vmax = Ip \cdot \sqrt{\frac{Lleak}{Clump}}$ (eq. 24) where Clump represents the total parasitic capacitance seen at the MOSFET opening.

Depending on the output power, you can either wire a simple capacitor across the MOSFET or an R–C network, as shown by Figure 32.

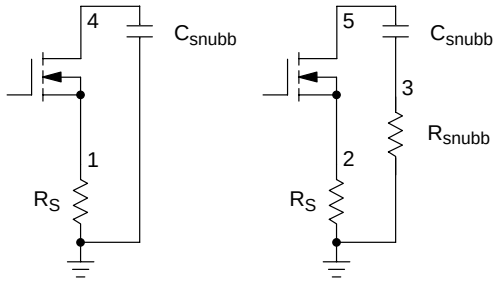

Figure 32. If the output power is low, you can wire a simple capacitor MOSFET's drain and ground

To calculate the values of this RC snubber, you need to measure the ringing frequency imposed by the leakage inductance and all the stray capacitances. Make sure you use a low capacitance probe, otherwise you might affect the observed frequency. Once you have it, calculate the impedance of the leakage inductance at the ringing frequency: $Z = 2 \cdot \pi \cdot Fring \cdot Lleak$ (eq. 25). Wiring a resistor R whose value equals Z should solve the problem but at the expense of a large power dissipation. To lower the dissipated heat, you can wire a capacitor C in series with R: $C = \frac{1}{\pi \cdot Fring \cdot R}$ (eq. 26). If the output power is low, you can directly wire this capacitor between the MOSFET drain and ground (not between drain–source to avoid substrate injection). Unfortunately, you discharge this capacitor in the MOSFET every time it turns on . . . Further tweaking is thus necessary to tune the dissipated power versus standby power.

ON Semiconductor Protection Devices

SMPS protection clearly needs fast switching components to ensure a reliable operation in the event of dangerous transients. ON Semiconductor portfolio offers a comprehensive list of semiconductors dedicated to protection: fast diodes, zeners, TVS etc. Below is a small list of typical component you can select to protect the MOSFET in your application. The complete list of TVS devices can be found at the following URL: *www.onsemi.com* or by ordering the selection guide TVSPROMO1299/D by sending an email to: ONlit@hibbertco.com:

Clipping Elements

Reference	Nominal Voltage (V)	Average Power (W)	Maximum Peak Power
1N5953B	150	1.5	98 W @ 1.0 ms
1N5955B	180	1.5	98 W @ 1.0 ms
1N5383B	150	5.0	180 W @ 8.3 ms
1N5386B	180	5.0	180 W @ 8.3 ms
1N5388B	200	5.0	180 W @ 8.3 ms
P6KE150A	150	5.0	600 W @ 1.0 ms
P6KE180A	180	5.0	600 W @ 1.0 ms
P6KE200A	200	5.0	600 W @ 1.0 ms
1.5KE150A	150	5.0	1.5 kW @ 1.0 ms
1.5KE180A	180	5.0	1.5 kW @ 1.0 ms
1.5KE200A	200	5.0	1.5 kW @ 1.0 ms

Fast Diodes

Reference	V_{RRM}	Ton (Typical)	IF Max
MUR160	600 V	50 ns	3.0 A
MUR1100E	1000 V	25 ns	3.0 A
1N4937	600 V	200 ns	1.0 A
MSR860*	600 V	100 ns	8.0 A
MSRB860–1*	600 V	100 ns	8.0 A

*Soft Recovery Diodes

Auxiliary Supply

As Figure 29 shows, we are using the auxiliary winding in a Forward mode. Further to what we have discussed, the auxiliary voltage will then be fixed by the primary/auxiliary turn ratio through the following formula: $Vcc = VHV \cdot \frac{Naux}{Np}$. We have to ensure full operation at low line (min Vcc = 8.0 V) and be sure to not trigger the internal SOFA OVP at high line (unless this becomes a safety recommendation against accidental high line levels). With line varying between 120 V and 350 VDC, the minimum turn ratio is 8/120 = 0.066. If we include a design safety margin of 15%, we end up with a turn ratio of 0.08. At high line, the level will rise up to: 350 x 0.08 = 28 V which is ok.

However, in standby, the switching frequency will largely diminish while the forward pulse become narrower. As a result, the Vcc capacitor refresh rate could be too low to ensure a correct level of self–supply at the lowest mains condition. We need to verify this point through calculation and simulation. At no–load we have:

Ipeak = Ip max/3.0 or 250 mV/Rsense = 138 mA. Including the 250 ns propagation delay, Ip = 157 mA

V_{out} = 6.5 V

VFB ≈ 3.0 V over 4.7 kΩ → optocoupler collector current ≈ 640 μA

Isecondary bias ≈ 640 μA with a Current Transfer Ratio (CTR) of 100%

Pout = 6.5 V x 640 μA = 4.0 mW.

The efficiency being rather low at these levels of power, experience shows that an input power around 40 mW including the MOSFET losses, ESR losses etc. is more realistic. Applying eq. 9, we can obtain an estimation of the switching frequency in standby: $\frac{Pin \cdot 2}{Lp \cdot Ip?} \approx 2.0\ kHz$. With a 120 VDC (low line) input level, the power MOSFET closes during: $\frac{1.55\ m \cdot 0.157}{120} = 2.0\ \mu s$. We can now feed our simulator with the calculated values: pulses of 0.08 x 120 = 9.6 V, lasting 2.0 μs and recurring with a 2.0 kHz frequency. Figure 33 shows the proposed simulation setup where the SOFA consumption is given by the 1.2 mA current source:

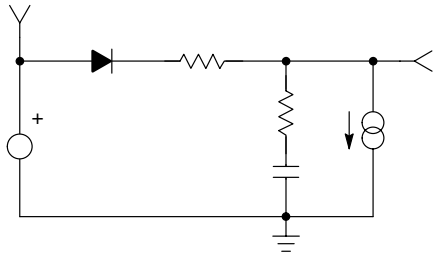

Figure 33. A simple simulation setup lets you evaluate the auxiliary Vcc level you will reach in standby

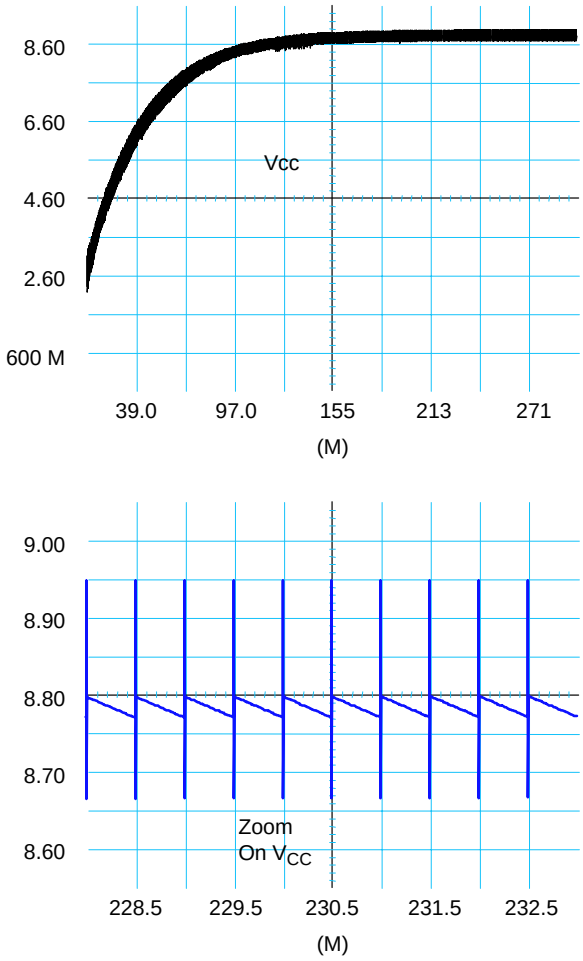

Figure 34. We have been obliged to raise the turn ratio in order to ensure an adequate Vcc level around 8.0 V

The simulation revealed a slightly low Vcc level at 120 VDC input line. Raising the auxiliary turn ratio from 0.08 up to 0.095 fixes the problem. In high line conditions, Vcc will go up to 350 x 0.095 = 33.3 V, lower than SOFA trip point. In case of over–voltage, the 36 V (min) SOFA trip point will stop the operation at a 267 VAC line level.

Final transformer specifications:

Lp = 1.55 mH
Np : Ns*power* = 1 : 0.08
Np : Ns*aux* = 1 : 0.095
Maximum primary peak current = 691 mA
Primary RMS current = 182 mA
Secondary RMS current = 2.53 A

Notes

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